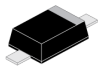
Silicon Epitaxial Planar Switching Diode

1N4148W
Package SOD-123(GW)
1N4148WFL
Package SOD-123FL




SOD123FL SOD123GW

Surface mount
Plastic Package
RoHS compliant

Device: 1N4148W, Package: SOD-123GW, marking code:**T4**

Device:1N4148WFL, Package: SOD-123FL, marking code: **W1**

FEATURES:

1. Fast Switching
2. These diodes are also available in other case style including the DO-35 case with the type designation 1N4148M, the MiniMELF case with the type designation LL4148 and the MicroMELF case type designation MCL4148.
3. This product is available in AEC-Q101 Qualified and PPAP Capable also.

Note: For AEC-Q101 qualified products, please use suffix -AQ in the part number while ordering.

Absolute Maximum Ratings (T_A = 25°C)

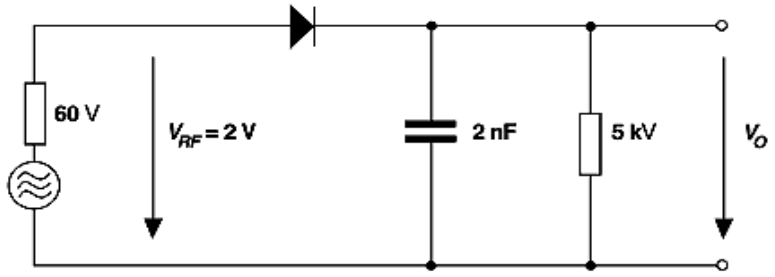
Parameter		Symbol	Value	Unit
Peak Reverse Voltage		V_{RM}	100	V
Reverse Voltage		V_R	75	V
Average Rectified Forward Current		$I_{F(AV)}$	150	mA
Non-repetitive Peak Forward Surge Current	at t = 1s	I_{FSM}	0.5	A
	at t = 1ms		1	
	at t = 1µs		4	
Power Dissipation		P_{tot}	400	mW
Thermal Resistance from Junction to Ambient Air		$R_{\theta JA}$	312	°C/W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS at T_a = 25 ℃

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Reverse Breakdown Voltage	$V_{(BR)}$	at I_R = 1 μA	75	--	--	V
Forward Voltage	V_F	at I_F = 1 mA	--	--	0.715	
		at I_F = 10 mA	--	--	0.855	
		at I_F = 50 mA	--	--	1.00	
		at I_F = 150 mA	--	--	1.20	
Peak Reverse Current	I_R	at V_R = 75 V	--	--	1	μA
		at V_R = 20 V	--	--	25	nA
		at V_R=75V @T_J 150℃	--	--	50	μA
		at V_R=25V@T_J 150℃	--	--	30	μA
Total Capacitance	C_T	at V_R = 0V, f = 1 MHz	--	--	2	pF
Reverse Recovery Time	t_{rr}	at I_F = 10mA, I_R = 1mA, V_R = 6V, R_L = 100Ω	--	--	4	nS

TEST CIRCUIT AND DIAGRAMS

Rectification Efficiency Measurement Circuit



TYPICAL CHARACTERISTICS CURVES

Fig 1: Forward Characteristics

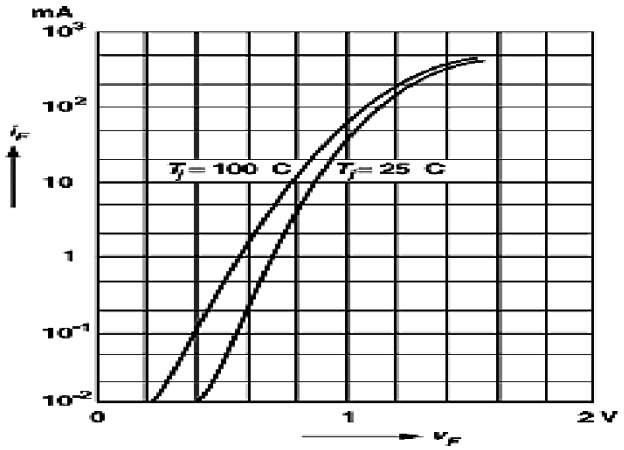


Fig 2: Admissible Power Dissipation Versus Ambient Temperature

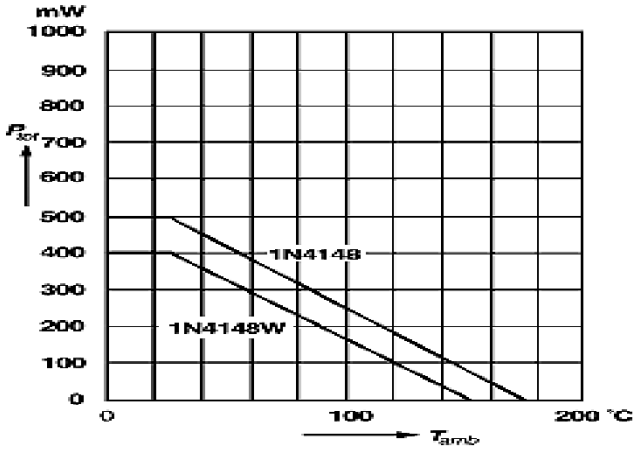


Fig 3: Dynamic Forward Resistance Versus Forward Current

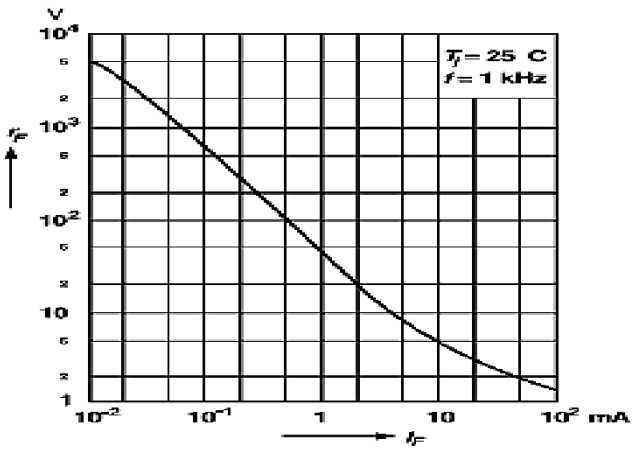
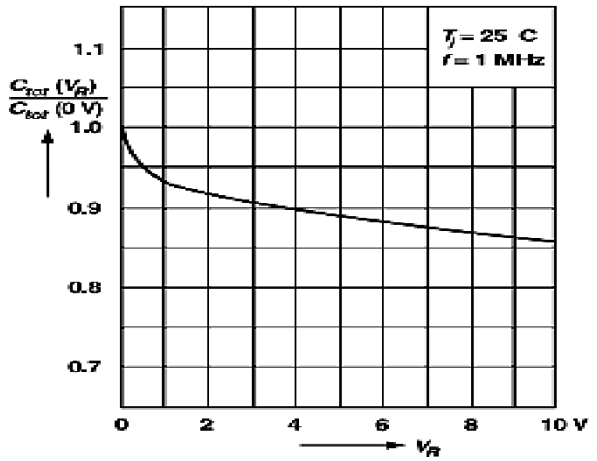


Fig 4: Relative Capacitance Versus Reverse Voltage



TYPICAL CHARACTERISTICS CURVES

Fig 5: Leakage Current Versus Junction Temperature

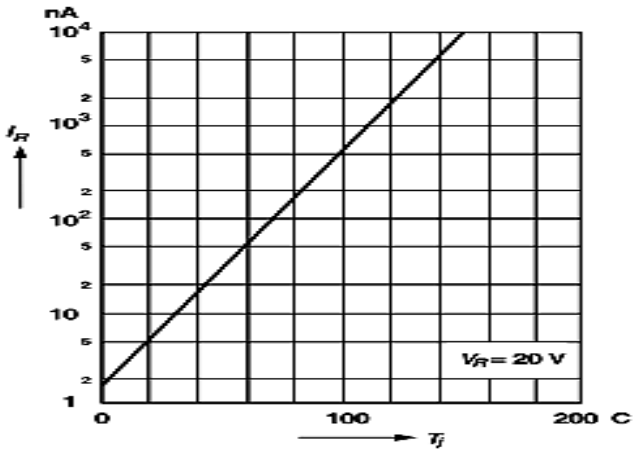
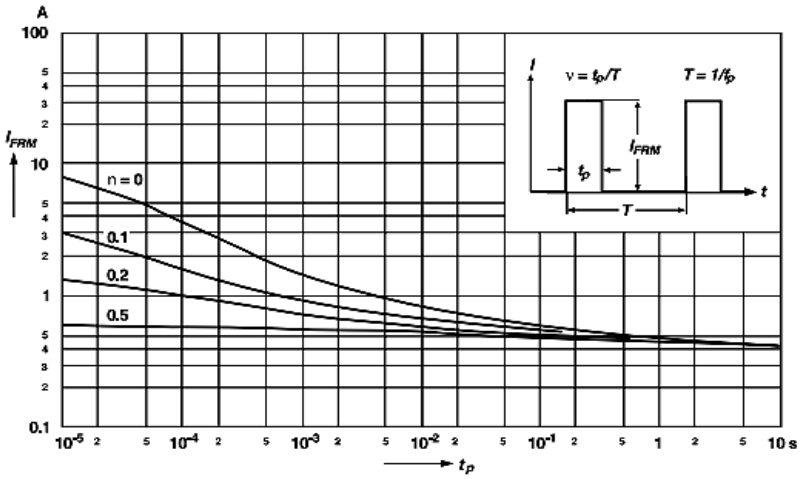
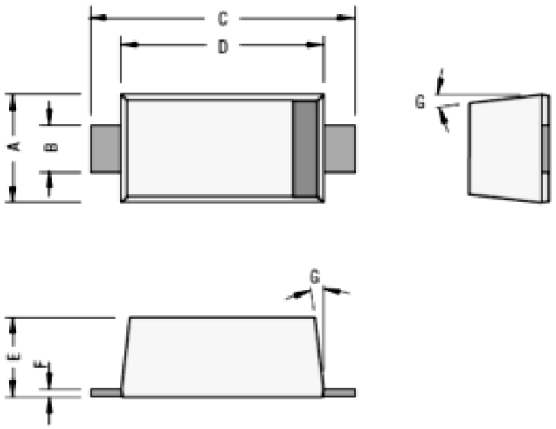


Fig 6: Admissible Repetitive peak Forward Current Versus Pulse Duration
For Condition,see Footnote in Table Absolute Maximum Ratings



Package Details

Package SOD123FL



DIM	Min	Max
A	1.55	1.65
B	0.50	0.60
C	3.70	3.90
D	2.60	2.70

DIM	Min	Max
E	1.05	1.15
F	0.127	0.135
G	5°	

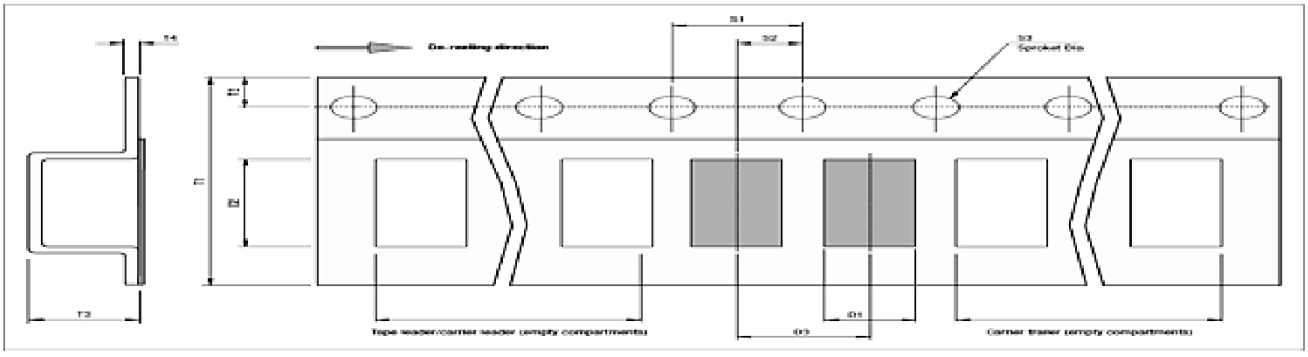
Cathode is marked by a Band

Packaging Specifications

T & A: Tape and Ammo Pack; **T & R:** Tape and Reel; **Bulk:** Loose in Poly Bags; **Tube:** Tube and Carton; **K:** 1,000

Package / Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
SOD-123FL	T & R	3,000	24K	18.5 x 18.5 x 10.5	1.0	120K	54.5 x 20.2 x 20.2	4.8

Packaging Tape Specifications for SMD Packages

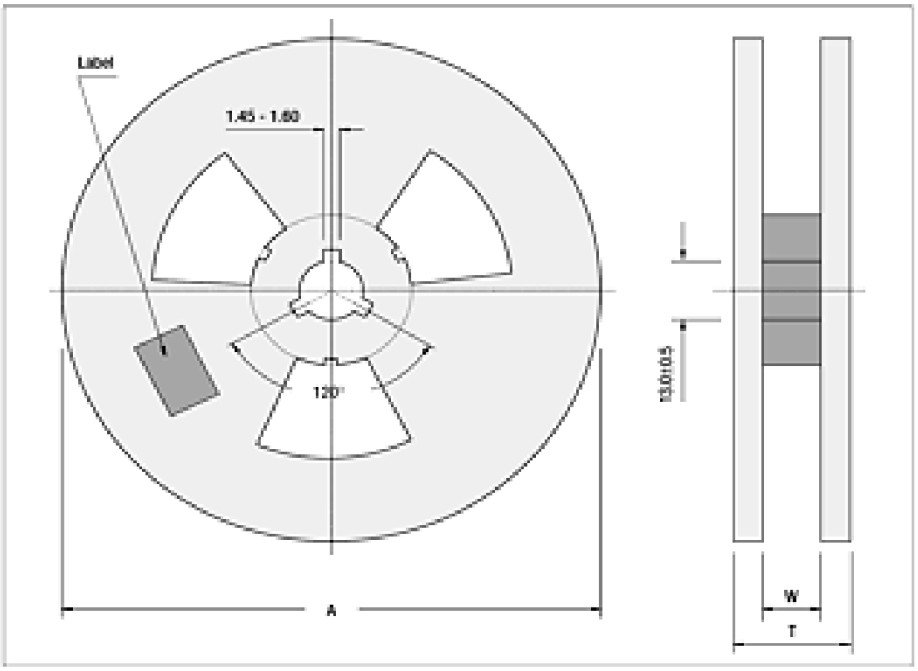


SMD Tape Specifications (8-12 mm)

Device	D1	D2	D3	T1	T2	T3 Max	T4 Max	S1	S2	S3 Dia
	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
SOD-123FL	2.0±0.1	3.9±0.1	4.0±0.1	8.3±0.1	1.75±0.1	1.66	0.28	4.0±0.1	2.0±0.1	1.5±0.1

All Dimensions are in mm

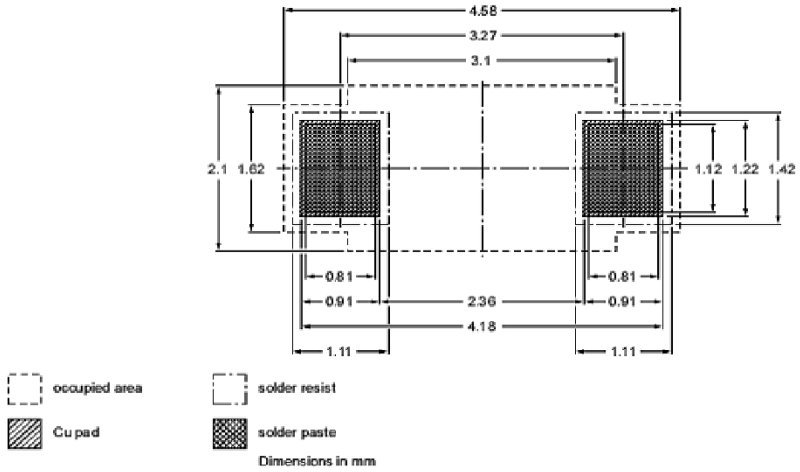
Reel Specifications for SMD Packages



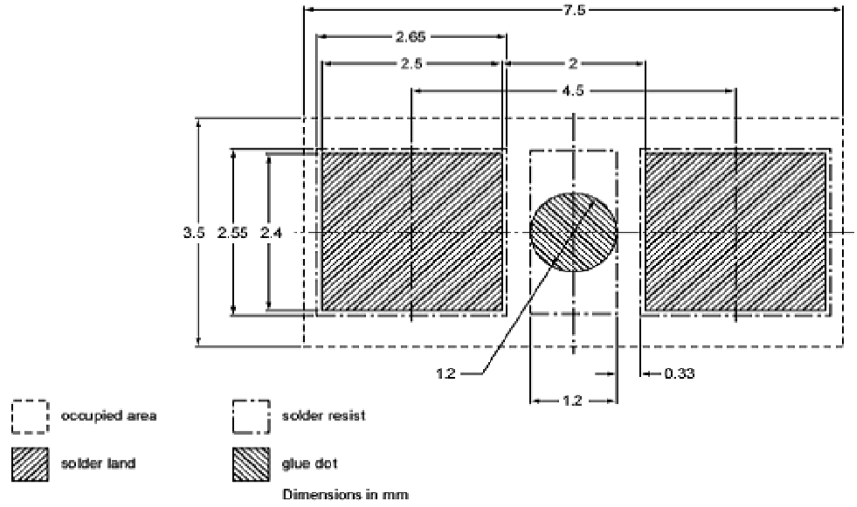
Reel Specifications

Package	Tape Width	Reel Dia. A - Max	Devices per Reel and MOQ	Inside Thickness W	Reel Thickness T - Max
SOD-123FL	8	180	3,000	8.4±2	14.4

Reflow soldering footprint for SOD123 FL

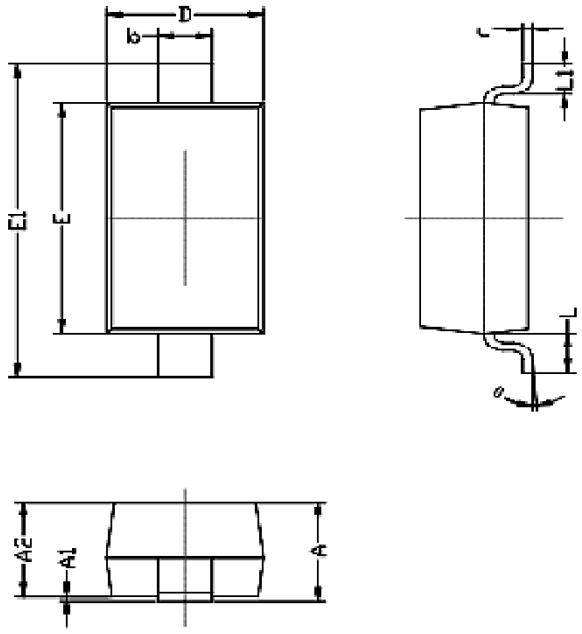


Wave soldering footprint for SOD123 FL



Package Details

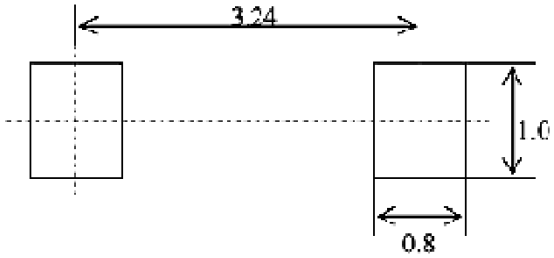
Package SOD123GW



SYMBOL	MIN(mm)	MAX(mm)
A	1.050	1.250
A1	0.000	0.100
A2	0.050	1.150
b	0.450	0.650
c	0.080	0.150
D	0.500	1.700
E	2.600	2.800
E1	3.550	3.850
L	0.500 REF	
L1	0.250	0.45
θ	0°	8°

All Dimensions are in mm

Recommended PCB pad layout



General Instructions:

1. Plastic package size: 2.70 X 1.60 sq. mm
2. General tolerances are: ±0.05mm

Center distance:	3.24
Foot width:	0.55
Pad width:	1.00
Foot length:	0.50
Pad length:	0.80

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

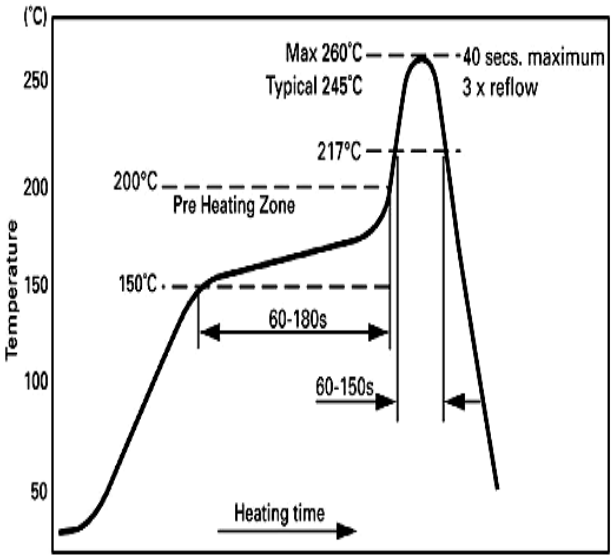
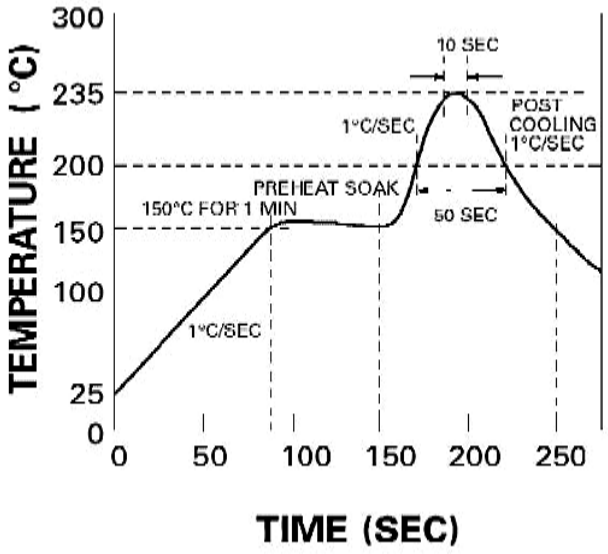


Figure 2

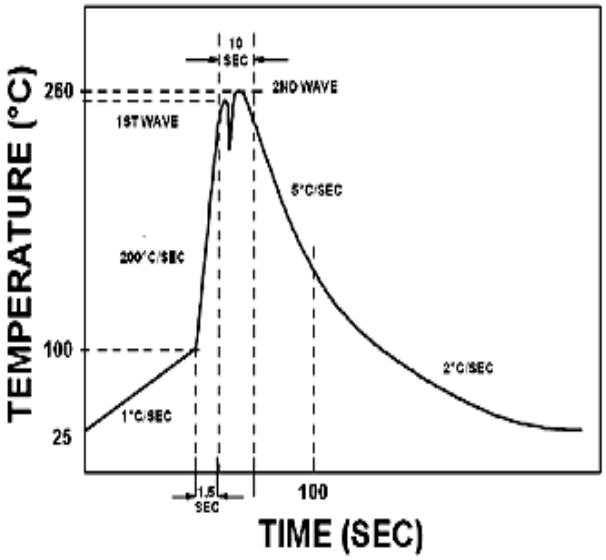


Reflow profiles in tabular form

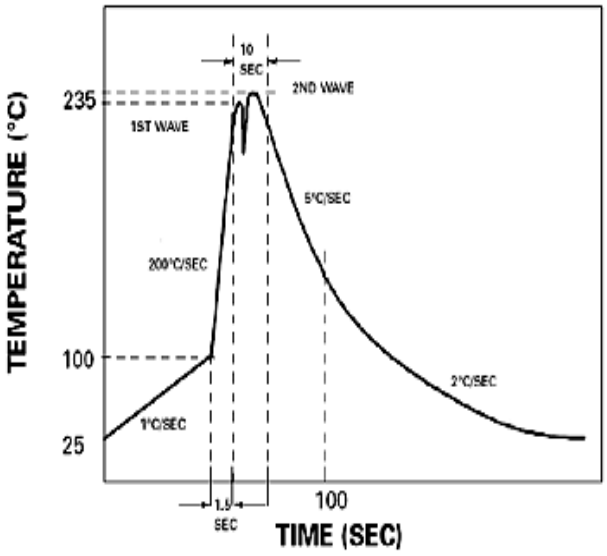
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Tim	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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