SILICON EPITAXIAL PLANAR ZENER DIODES

1N4614~1N4627

DO-35

DO-35
Axial Leaded
Glass Package
RoHS compliant

ABSOLUTE MAXIMUM RATINGS [1] (Ta = 25°C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Operating Temperature	T_{STG}	-65 to +175	°C
DC Power Dissipation @ 50°C	P_D	500	mW
Power Derating above 50°C		4.0	mW
Forward Voltage 1.1 Volts maximum	V_F	200.0	mA

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

TYPE NUMBER	Nominal Zener Voltage V_Z @ I_{ZT} (Note 1)	Zener Test Current I_{ZT}	Maximum Zener Impedance Z_{ZT} @ I_{ZT} (Note 2)	Maximum Reverse Leakage Current 1_R @ V_R		Maximum DC Zener Current I_{ZM}	Maximum Noise Density N_D
	V	µA	Ω	µA	V	mA	µV/Hz
1N4614	1.8	250	1200	7.5	1	120	1
1N4615	2.0	250	1250	5.0	1	110	1
1N4616	2.2	250	1300	4.0	1	100	1
1N4617	2.4	250	1400	2.0	1	95	1
1N4618	2.7	250	1500	1.0	1	90	1
1N4619	3.0	250	1600	0.8	1	87	1
1N4620	3.3	250	1650	7.5	1.5	85	1
1N4621	3.6	250	1700	7.5	2	83	1
1N4622	3.9	250	1650	5.0	2	80	1
1N4623	4.3	250	1600	4.0	2	77	1
1N4624	4.7	250	1550	10.0	2	75	1
1N4625	5.1	250	1500	10.0	2	70	2
1N4626	5.6	250	1400	10.0	2	65	4
1N4627	6.2	250	1200	10.0	2	61	5

Note:

1. The type numbers shown above have a Zener voltage tolerance of + 5% of the nominal Zener voltage. V is measured with the device junction in thermal equilibrium at an ambient temperature of 25°C + 3°C. A “C” suffix denotes a + 2% tolerance and a “D” suffix denotes a + 1% tolerance.
2. Zener impedance is derived by superimposing on I_{ZT} A 60Hz rms a.c. current equal to 10% of I Z_T (25µA a.c.)

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

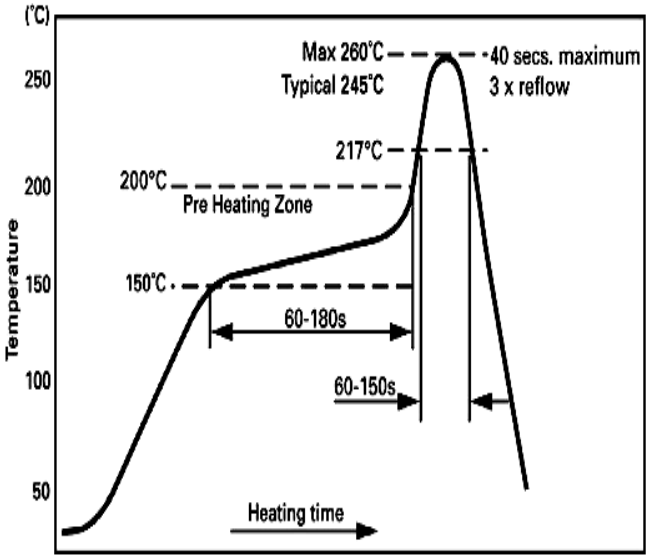
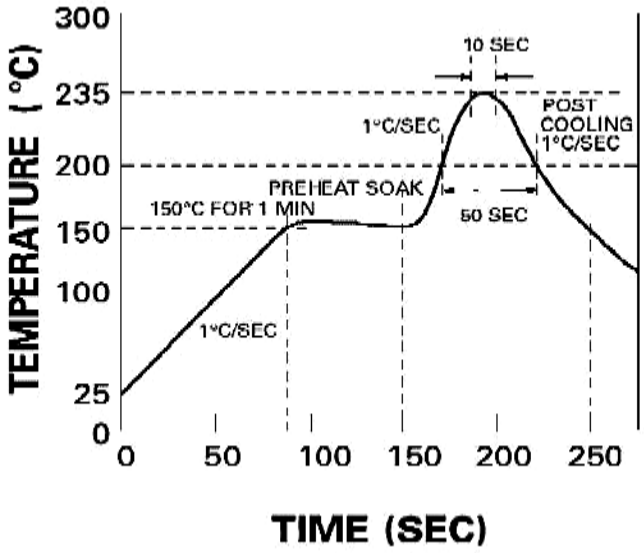


Figure 2

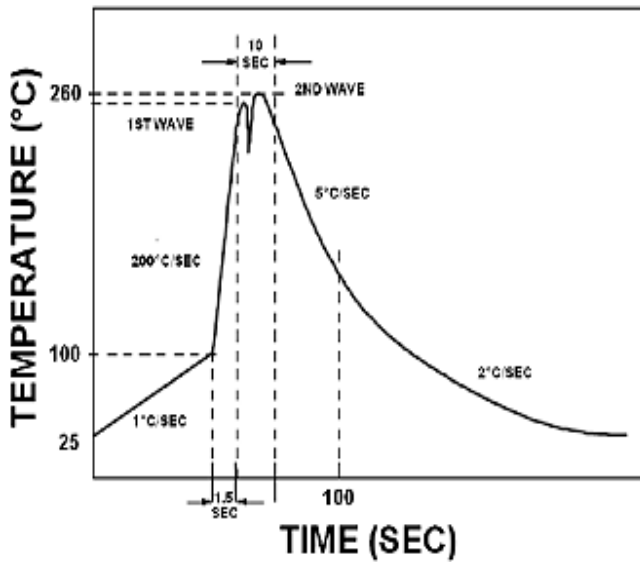


Reflow profiles in tabular form

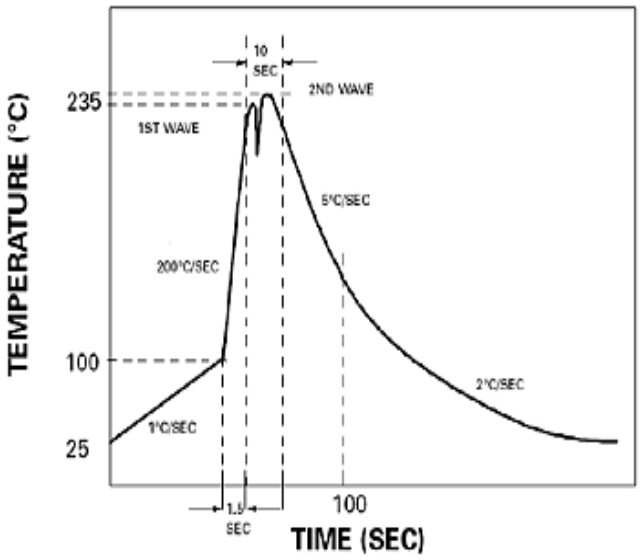
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: Typical Thermal Resistance

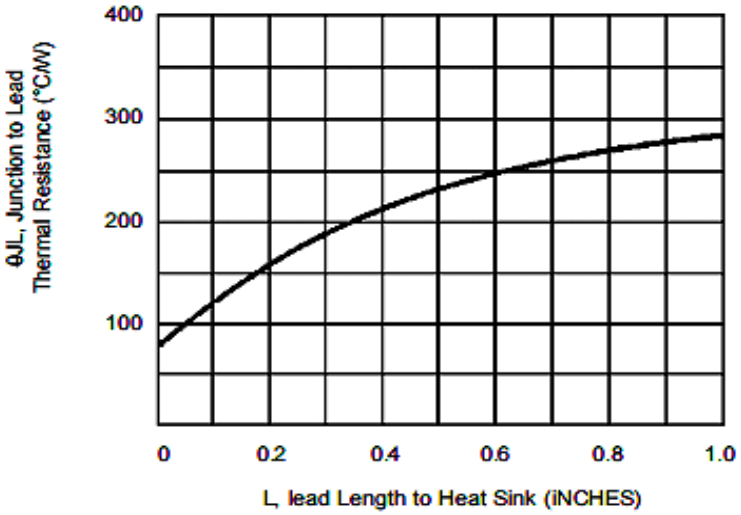
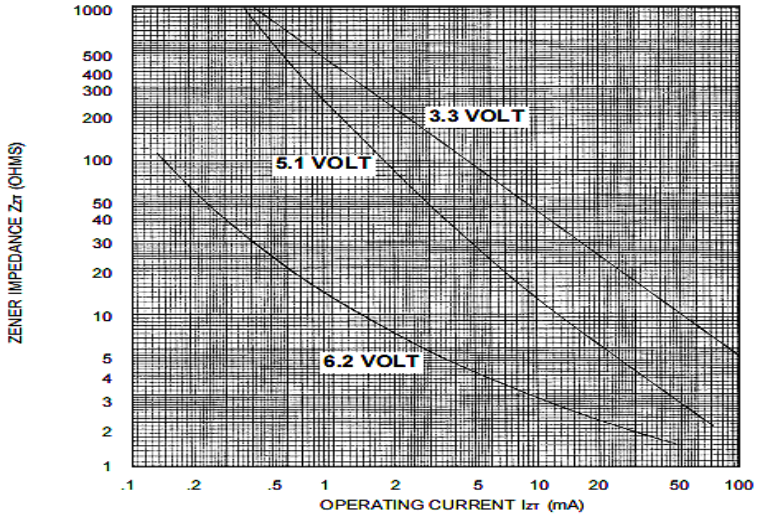
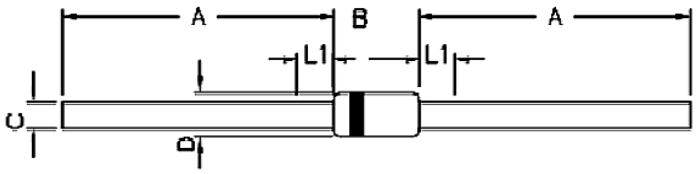


Fig 2: Zener Impedance's Operating Current



PACKAGE DETAILS

DO-35 Glass Axial Package



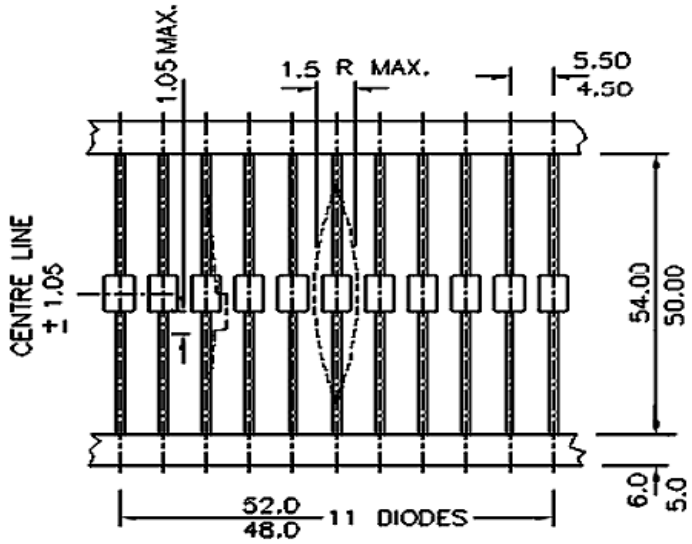
Note:

Cathode is Marked by Band

DIM	MIN	MAX
A	25.40	38.10
B	3.05	5.08
C	0.46	0.55
D	1.53	2.28
L1	--	1.27

All Dimensions are in mm

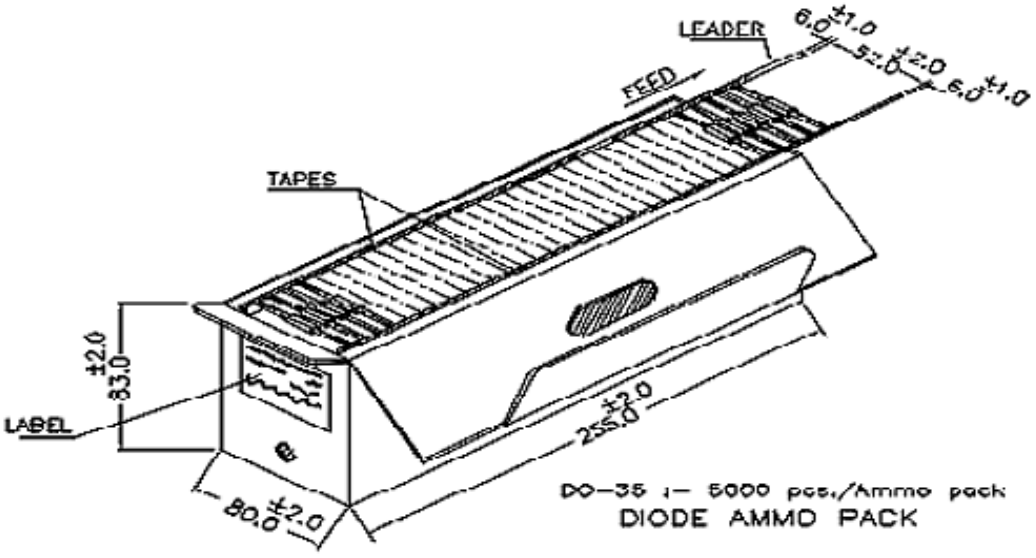
DO-35, 52mm Taping Specification



52mm Taping Specification

1. T & A Indicates Axial Tape & Ammo Packing (52 mm Tape Spacing)
2. 300 mm(min) leader tape on everyspool
3. No. of empty places allowed 0.25% without Consecutive empty places
4. Ends of leads shall preferably not protrude beyond the tapes
5. Components shall be help sufficiently in the tape or tapes so that they can not come free in normal

All Dimensions are in mm



on request also available in 26 mm Tape and Ammo Pack

Packing Details

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Qty
DO-35 T&A	5K/ammo box	0.88kg/5K pcs	10"X3.5"X3.5"	5.0K	12.7"X12.7"X20"	125.0K	25Kgs

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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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