# NPN SILICON PLANAR EPITAXIAL SWITCHING TRANSISTORS

TO-92

**2N3903**
**2N3904**

**TO-92**
**Plastic Package**
**RoHS compliant**

## FEATURE:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

**Note:** For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

**APPLICATIONS:** General Purpose Switching And Amplifier Applications

## ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Collector Emitter Voltage | $V_{CEO}$ | 40 | V |
| Collector Base Voltage | $V_{CBO}$ | 60 | V |
| Emitter Base Voltage | $V_{EBO}$ | 6.0 | V |
| Collector Current Continuous | $I_C$ | 200 | mA |
| Power Dissipation at Ta=25ºC | $P_D$ | 625 | mW |
| Derate Above 25ºC | | 5.0 | mW/°C |
| Power Dissipation at Tc=25ºC | $P_D$ | 1.5 | W |
| Derate Above 25ºC | | 12 | mW/°C |
| Operating and Storage Junction Temperature Range | $T_j$, $T_{stg}$ | -55 to +150 | °C |

## THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| Junction to Case | $R_{th\ (j\text{-}c)}$ | 83.3 | °C/W |
| Junction to Ambient in free air | $R_{th\ (j\text{-}a)}$ | 200 | °C/W |

## ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | Min/ Max | 2N3903 | 2N3904 | UNIT |
|---|---|---|---|---|---|---|
| Collector Emitter Voltage | $V_{CEO}$ | $I_C$=1mA, $I_B$=0 | Min | 40 | | V |
| Collector Base Voltage | $V_{CBO}$ | $I_C$=10m A. $I_E$=0 | Min | 60 | | V |
| Emitter Base Voltage | $V_{EBO}$ | $I_E$=10m A, $I_C$=0 | Min | 6.0 | | V |
| Base Cut Off Current | $I_{BL}$ | $V_{CE}$=30V, $V_{EB}$=3V | Max | 50 | | nA |
| Collector Cut Off Current | $I_{CEX}$ | $V_{CE}$=30V, $V_{EB}$=3V | Max | 50 | | nA |

## ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | Min/ Max | 2N3903 | 2N3904 | UNIT |
|---|---|---|---|---|---|---|
| DC Current Gain | $h_{FE}$ [1] | $I_C$=0.1mA, $V_{CE}$=1V | Min | 20 | 40 | |
| | | $I_C$=1mA, $V_{CE}$=1V | Min | 35 | 70 | |
| | | $I_C$=10mA, $V_{CE}$=1V | | 50~150 | 100~300 | |
| | | $I_C$=50mA, $V_{CE}$=1V | Min | 30 | 60 | |
| | | $I_C$=100mA, $V_{CE}$=1V | Min | 15 | 30 | |
| Collector Emitter Saturation Voltage | $V_{CE\ (sat)}$ [1] | $I_C$=10mA, $I_B$=1mA | Max | 0.2 | | V |
| | | $I_C$=50mA, $I_B$=5mA | Max | 0.3 | | V |
| Base Emitter Saturation Voltage | $V_{BE\ (sat)}$ [1] | $I_C$=10mA, $I_B$=1mA | | 0.65~0.85 | | V |
| | | $I_C$=50mA, $I_B$=5mA | Max | 0.95 | | V |
| Transistors Frequency | $f_T$ | $I_C$=10mA, $V_{CE}$=20V, f=100MHz | Min | 250 | 300 | MHz |
| Output Capacitance | $C_{ob}$ | $V_{CB}$=5V, $I_E$=0, f=1MHz | Max | 4.0 | | pF |
| Input Capacitance | $C_{ib}$ | $V_{EB}$=0.5V, $I_C$=0, f=1MHz | Max | 8.0 | | pF |
| **ALL TEST CONDITION f=1kHz** | | | | | | |
| Small Signal Current Gain | $h_{fe}$ | $I_C$=1mA, $V_{CE}$=10V | | 50~200 | 100~400 | |
| Input Inpedence | $h_{ie}$ | $I_C$=1mA, $V_{CE}$=10V | | 1.0~1.8 | 1.0~1.10 | kΩ |
| Voltage Feedback Ratio | $h_{re}$ | $I_C$=1mA, $V_{CE}$=10V | | 0.1~0.5 | 0.5~8 | x10 $^{-4}$ |
| Out put Admittance | $h_{oe}$ | $I_C$=1mA, $V_{CE}$=10V | | 1.0~40 | | μmhos |
| Noise Figure | $N_F$ | $I_C$=100m A, $V_{CE}$=5V, f=1KHz, RS=1KW | Max | 6.0 | 5.0 | dB |
| **SWITCHING Time** | | | | | | |
| Delay time | $t_d$ | $V_{CC}$=3V, $V_{BE}$=0.5V $I_C$=10mA, $I_{B1}$=1mA | Max | 35 | | ns |
| Rise time | $t_r$ | | Max | 35 | | ns |
| Storage time | $t_s$ | $V_{CC}$=3V, $I_C$=10mA $I_{B1}$=$1_{B2}$=1mA | Max | 175 | 200 | ns |
| Fall time | $t_f$ | | Max | 50 | | ns |

**Note:**

1. Pulse Condition: =300μs, Duty Cycle=2%

## Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

**Figure 1**

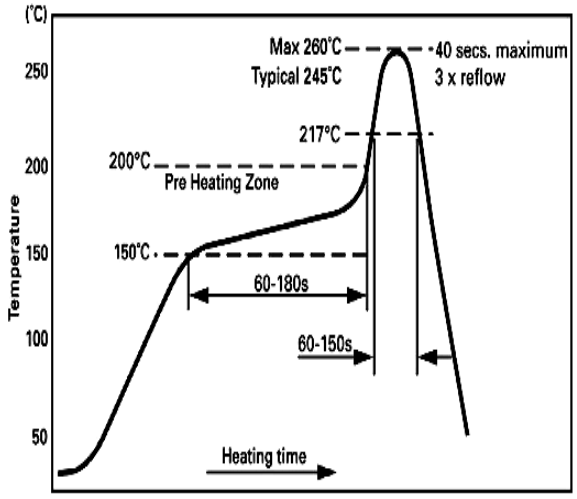
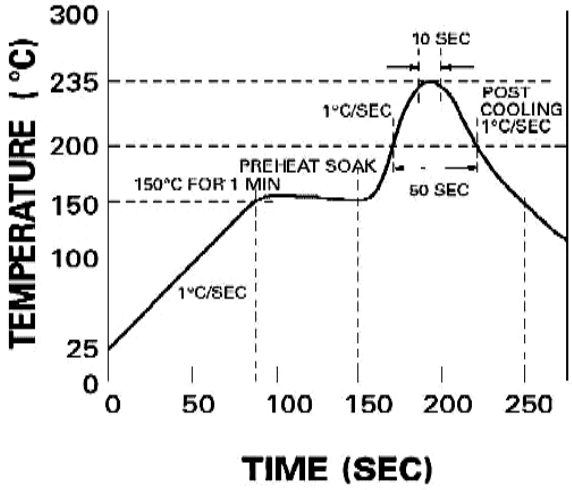



**Figure 2**

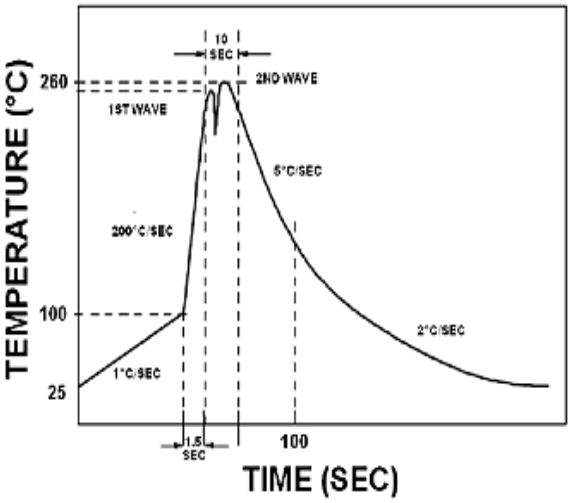



**Reflow profiles in tabular form**

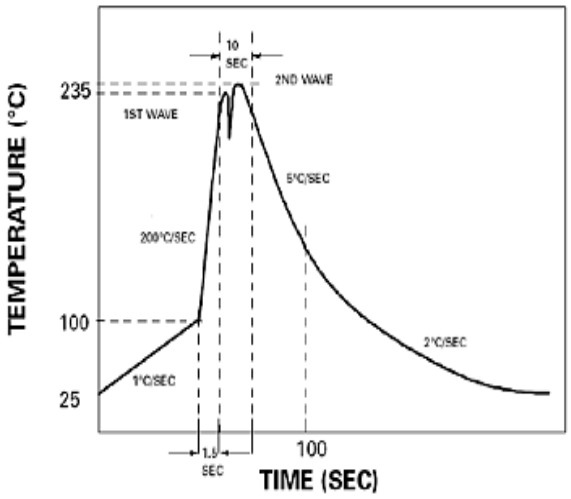
| Profile Feature | Sn-Pb System | Pb-Free System |
|---|---|---|
| Average Ramp-Up Rate | ~3°C/second | ~3°C/second |
| **Preheat**<br>– Temperature Range<br>– Time | <br>150-170°C<br>60-180 seconds | <br>150-200°C<br>60-180 seconds |
| Time maintained above:<br>– Temperature<br>– Time | <br>200°C<br>30-50 seconds | <br>217°C<br>60-150 seconds |
| Peak Temperature | 235°C | 260°C max. |
| Time within +0 -5°C of actual Peak | 10 seconds | 40 seconds |
| Ramp-Down Rate | 3°C/second max. | 6°C/second max. |

## Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used




The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder




### Wave Profiles in Tabular Form

| Profile Feature | Sn-Pb System | Pb-Free System |
|---|---|---|
| Average Ramp-Up Rate | ~200°C/second | ~200°C/second |
| Heating rate during preheat | Typical 1-2, Max 4°C/sec | Typical 1-2, Max 4°C/Sec |
| Final preheat Temperature | Within 125°C of Solder Temp | Within 125°C of Solder Temp |
| Peak Temperature | 235°C | 260°C max. |
| Time within +0 -5°C of actual Peak | 10 seconds | 10 seconds |
| Ramp-Down Rate | 5°C/second max. | 5°C/second max |

## TYPICAL CHARACTERISTICS CURVES

Fig 1: Capacitance

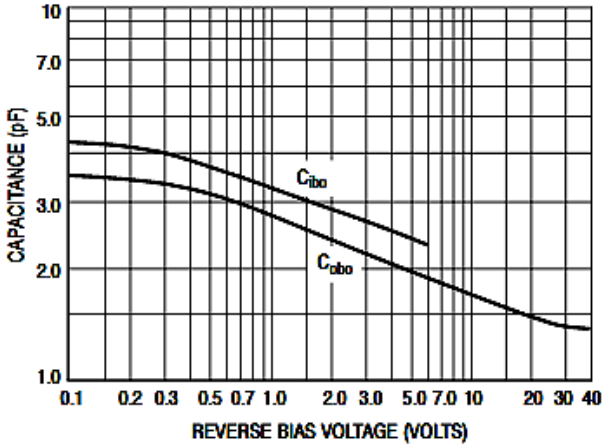



Fig 2: Turn −On Time

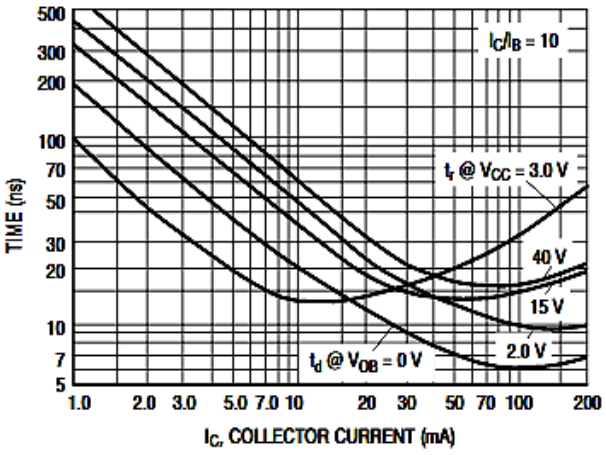



Fig 3: Storage Time

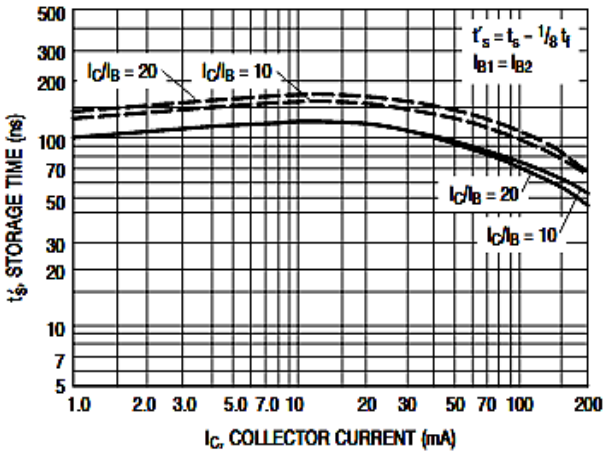



Fig 4: Charge Data

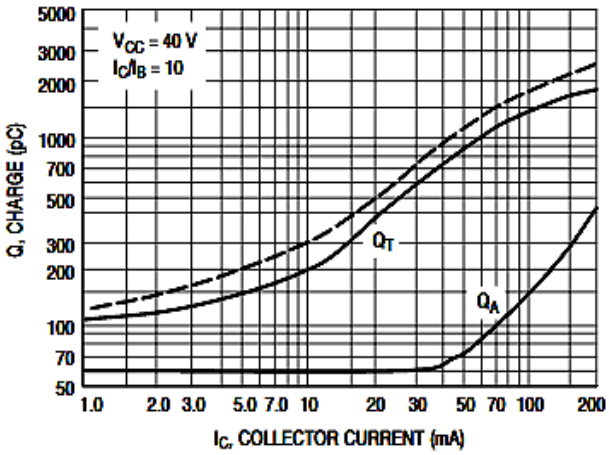



Fig 5: Rise Time

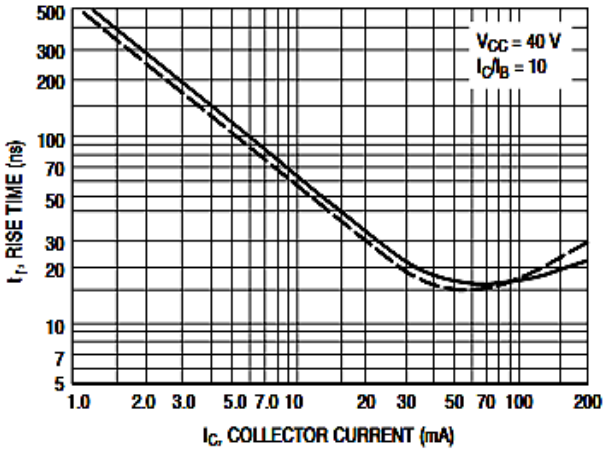
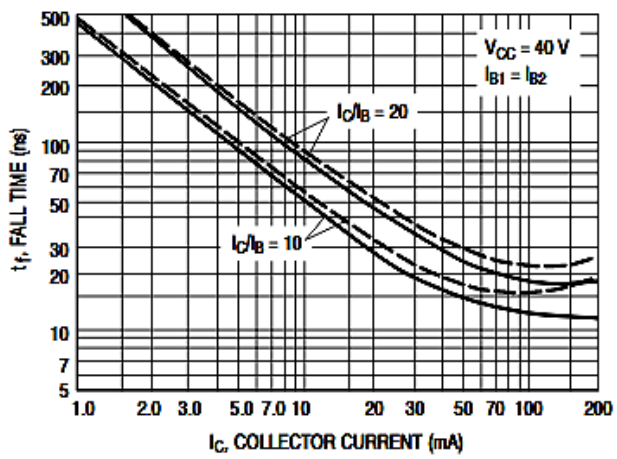



Fig 6: Fall Time

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## TYPICAL CHARACTERISTICS CURVES

Fig 7: Noise Figure Variation

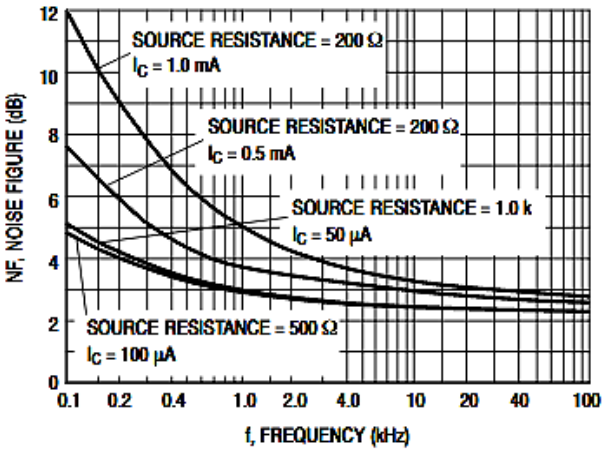



Fig 8: Current Gain

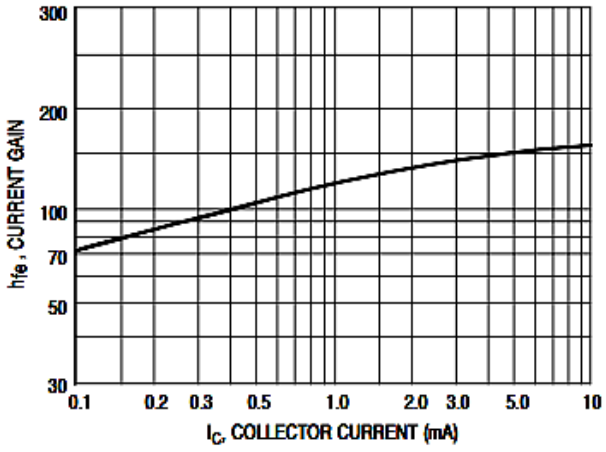



Fig 9: Input Impedance

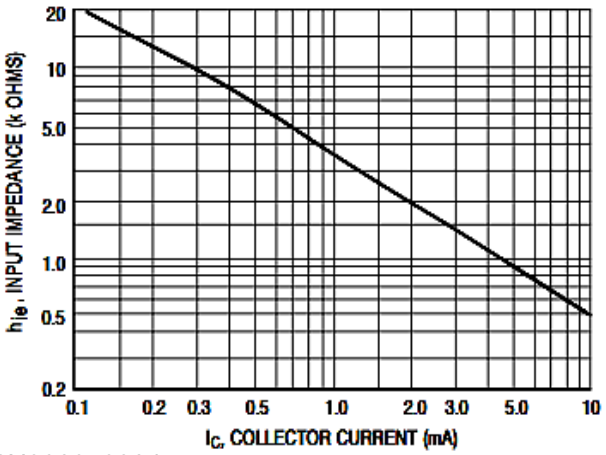



Fig 10: Noise Figure Variation

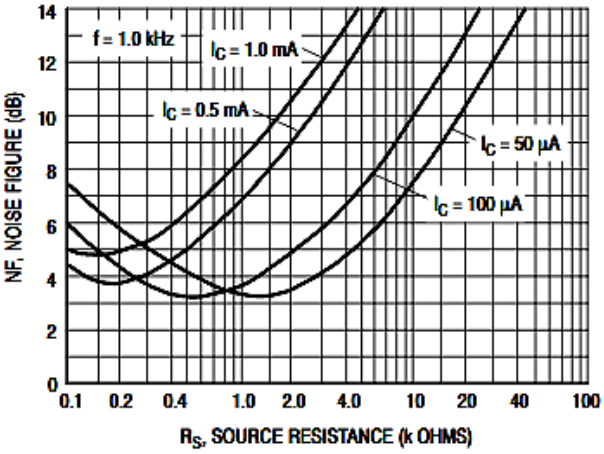



Fig 11: Output Admittance

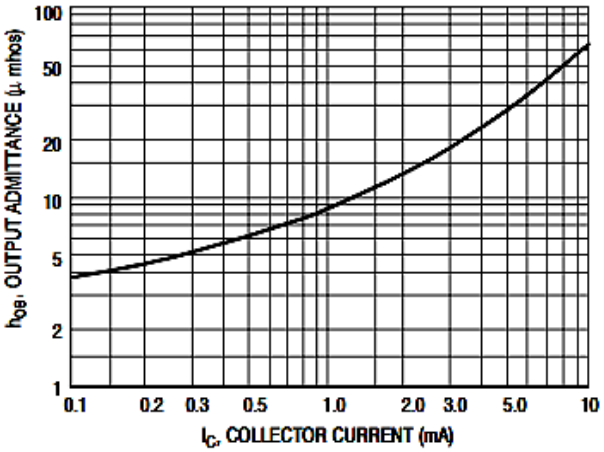
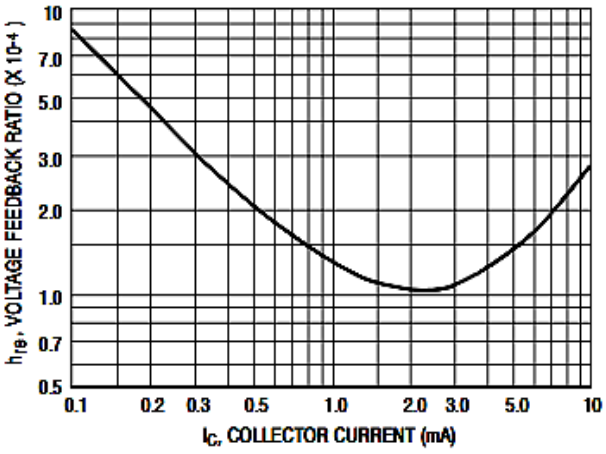



Fig 12: Voltage Feedback Ratio

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## TYPICAL CHARACTERISTICS CURVES

Fig 13: “ON” Voltages

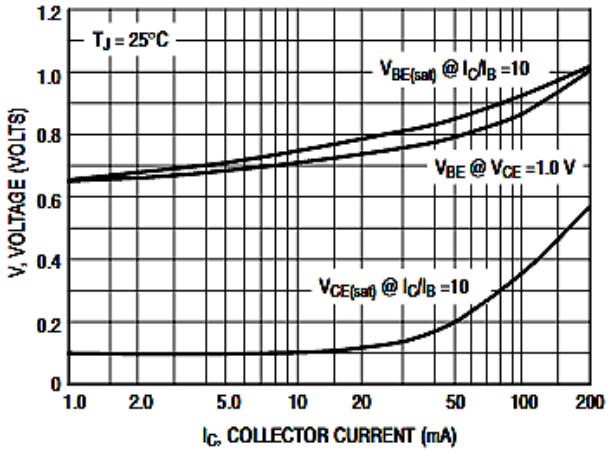



Fig 14: Temperature Coefficients

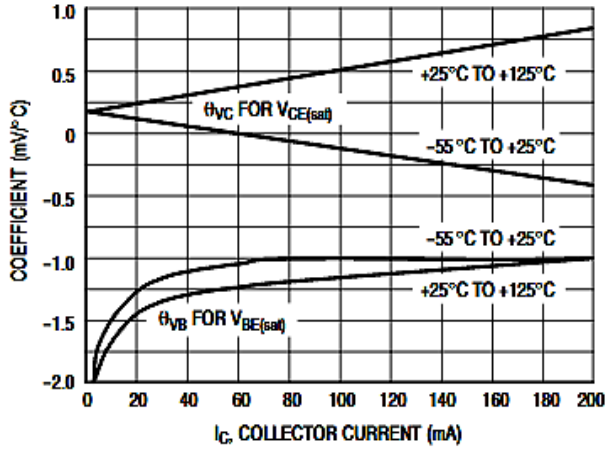



Fig 15: DC Current Gain

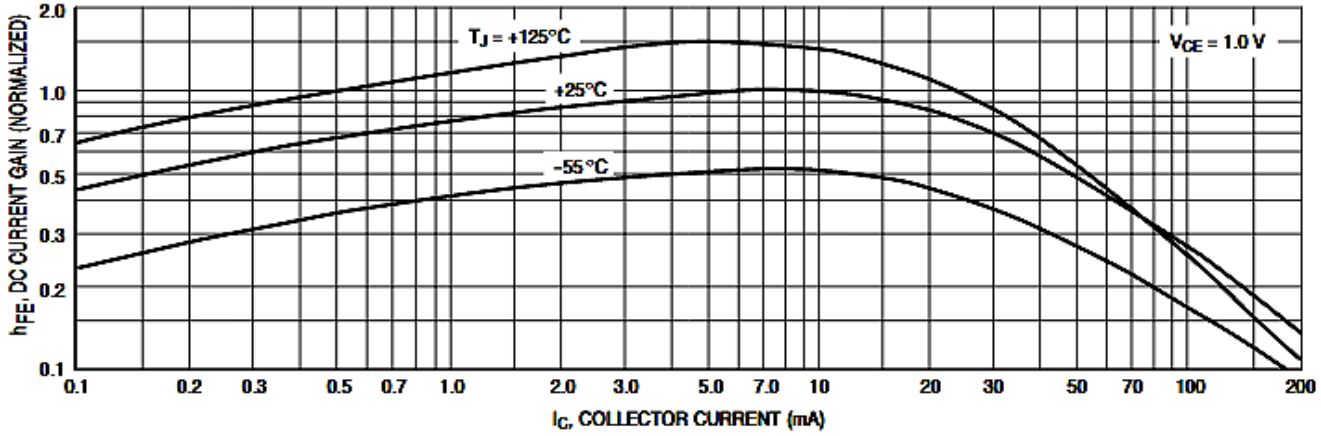
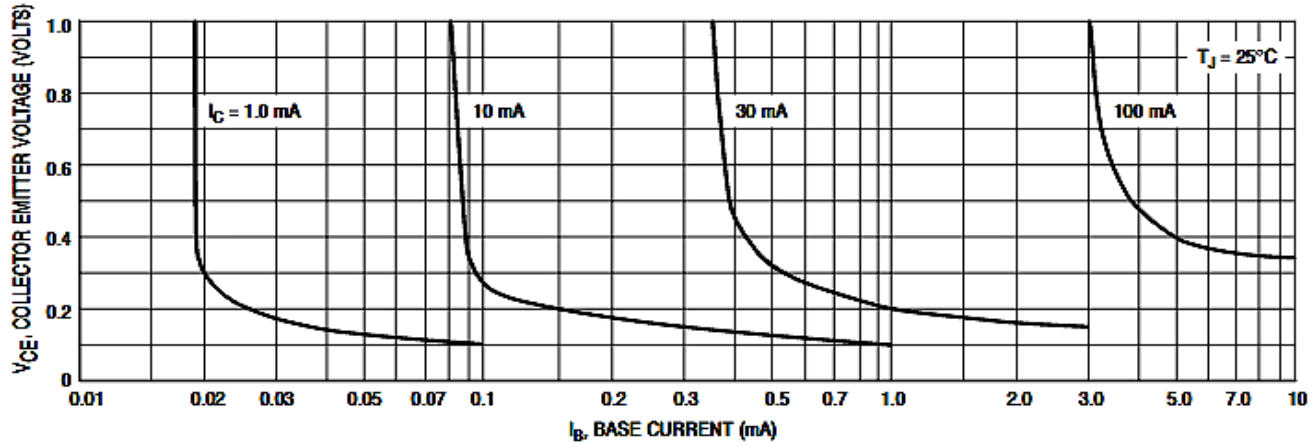
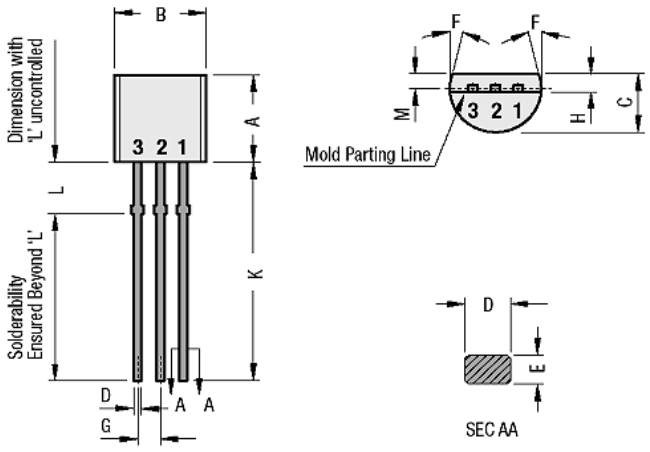



Fig 16: Collector Saturation Region



## PACKAGE DETAILS

TO-92 Leaded Plastic Package




| DIM | MIN | MAX |
|---|---|---|
| A | 4.32 | 5.33 |
| B | 4.45 | 5.20 |
| C | 3.18 | 4.19 |
| D | 0.40 | 0.55 |
| E | 0.30 | 0.55 |
| F | 5° | |
| G | 1.14 | 1.40 |
| H | 1.20 | 1.80 |
| K | 12.5 | |
| L | 1.982 | 2.082 |
| M | 1.030 | 1.530 |

All dimensions are in mm

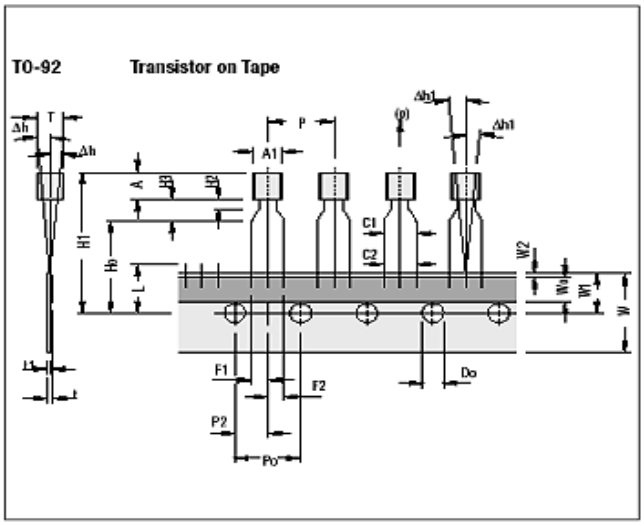
### PIN CONFIGURATION

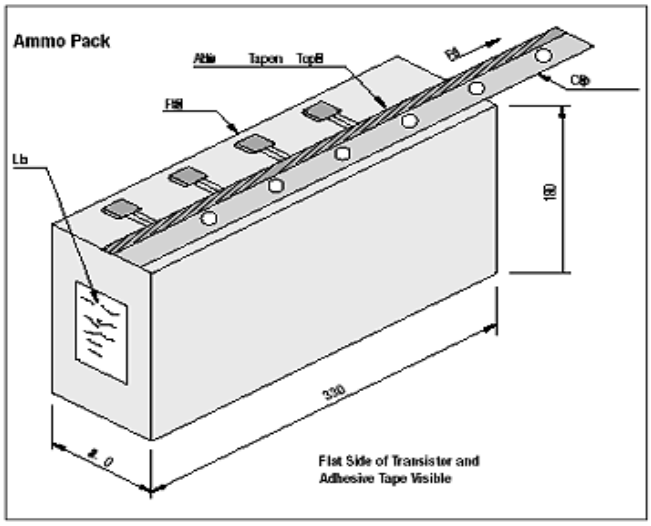
1. Collector
2. Base
3. Emitter

## Packaging Information

| Package/Case Type | Packaging Type | Std. Packing | Inner Carton | | | Outer Carton | | |
|---|---|---|---|---|---|---|---|---|
| | | Qty | Qty | Size L x W x H (cm) | Gross Weight (Kg) | Qty | Size L x W x H (cm) | Gross Weight (Kg) |
| TO-92 | Bulk | 1,000 | 5K | 19x19x8 | 1.10 | 80K | 43x40x35 | 20.0 |
| | T&A | 2,000 | 2K | 32x4.5x20 | 0.70 | 40K | 43x40x35 | 15.20 |

TO-92 Tape and Ammo Packaging




All Dimensions are in mm

## Tape Specifications

| Item description | Symbol | TO-92 Min | TO-92 Nom | TO-92 Max | TO-92 Tol |
|---|---|---|---|---|---|
| Body width | A1 | 4.45 | | 5.20 | |
| Body height | A | 4.32 | | 5.33 | |
| Body thickness | T | 3.18 | | 4.19 | |
| Pitch of component[Cr] | P | | 12.7 | | ±1.0 |
| Feed hole pitch[§1] | Po | | 12.7 | | ±0.3 |
| Feed hole center to component centre[§2] | P2 | | 6.35 | | ±0.4 |
| Comp. alignment, Side view[§3] | Dh | | 0 | 1.0 | |
| Comp. alignment, Front view[§3] | Dh1 | | 0 | 1.3 | |
| Tape width[Cr] | W | | 18 | | ±0.5 |
| Hold down tape width[Cr] | Wo | | 6 | | ±0.2 |
| Hole position | W1 | | 9 | | +0.7 -0.5 |
| Hold-down tape position | W2 | 0.0 | | 0.7 | |
| Lead wire clinch height | Ho | | 16 | | ±0.5 |
| Component height | H1 | | | 24.0 | |
| Length of snipped leads | L | | | 11.0 | |
| Feed hole diameter[Cr] | Do | | 4 | | ±0.2 |
| Total tape thickness[§4] | t | | | 1.2 | |
| Lead-to-lead distance[Cr] | F1, F2 | 2.4 | | 2.7 | |
| Stand off | H2 | 0.45 | | 1.45 | |
| Clinch height | H3 | | | 3.0 | |
| Lead parallelismCr | C1-C2 | | | 0.22 | |
| Pull-out force | (p) | 6N | | | |

**Taping Specification**

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.
§2 To be measured at bottom of clinch.
§3 At top of body.
§4 t1 = 0.3 – 0.6 mm
Cr Critical Dimension.

All Dimensions are in mm

# Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

## Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

## Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

| JEDEC MSL Level | | |
|---|---|---|
| **Level** | **Time** | **Condition** |
| 1 | Unlimited | ≤30 °C / 85% RH |
| 2 | 1 Year | ≤30 °C / 60% RH |
| 2a | 4 Weeks | ≤30 °C / 60% RH |
| 3 | 168 Hours | ≤30 °C / 60% RH |
| 4 | 72 Hours | ≤30 °C / 60% RH |
| 5 | 48 Hours | ≤30 °C / 60% RH |
| 5a | 24 Hours | ≤30 °C / 60% RH |
| 6 | Time on Label(TOL) | ≤30 °C / 60% RH |

## Customer Notes

**Component Disposal Instructions**

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

## Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.

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2N3903_3904
Rev02_25082022EM