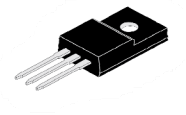
Sensitive gate SCR

BT258X



TO-220FP

TO-220FP
Fully Isolated
Plastic Package
RoHS compliant

DISCRIPTION:

The BT258X SCR is suitable to fit all models of control found in applications such as phase control, heating control, voltage regulation circuits.

FEATURES:

1. High blocking voltage
2. Low on-state voltage and high I_{TSM}
3. High heat dissipation and durability
4. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Repetitive Peak Off-State Voltage	V_{DRM}	BT258X - 600/800		600/800	V
Repetitive Peak Reverse Voltage	V_{RRM}			600/800	
Average on-state current	$I_{T(AV)}$	Half sine wave, T_{amb}<109°C		5	A
On-State RMS Current	$I_{T(RMS)}$	All conduction angles		8	A
Non Repetitive Surge Peak On-State Current	I_{TSM}	Full Sine wave, T_j=25°C, t=10ms		75	A
I^2t Value for Fusing	I^2t	t=10ms		28	A^2s
Repetitive Rate of Rise of On-State Current after Triggering	di/dt	T_M=20A, I_G=0.2A, dIG/dt=0.2A/µs		50	A/µs
Peak Gate Current	I_{GM}			2	A
Peak gate power	P_{GM}			5	W
Average Gate Power	$P_{G(AV)}$	Over any 20ms period		0.5	W
Storage Temperature	T_{stg}		-40	150	°C
Operation Junction Temperature	T_J			125	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance, Junction to Case	R_{thJ-C}			5.0	°C/W
Thermal Resistance, Junction to Ambient	R_{thJ-A}		55.0		

ELECTRICAL CHARACTERISTICS (T_A = 25°C; unless otherwise specifie

PARAMETER	SYMBOL	TEST CONDITION	Value			Unit
			Min.	Typ.	Max.	
Peak Repetitive Forward Blocking Current	I_{DRM}	$V_{DM}=V_{DRM(MAX)}$; T_j=125°C	-	0.1	0.5	mA
Peak Repetitive Reverse Blocking Current	I_{RRM}	$V_{RM}=V_{RRM(MAX)}$; Tj=125°C	-	0.1	0.5	mA
Peak On-State Voltage	V_{TM}	I_{TM}=16A	-	1.3	1.7	V
Gate Trigger Current	I_{GT}	V_{DM}=12V, I_T=0.1A	-	50	200	µA
Gate Trigger Voltage	V_{GT}	V_{DM}=12V, R_L=33Ω	-	0.4	1.5	V
Holding Current	I_H	V_{DM}=12V, I_{GT}=0.1A	-	0.3	6	mA
Latching Current	I_L	V_{DM}=12V, I_{GT}=0.1A	-	0.4	10	mA
Rise of Off-State Voltage	dV/dt	V_{DM}=67% $V_{DRM(MAX)}$, T_j=125°C Gate Open	50	100	-	V/µs
Gate controlled turn-on time	t_{gt}	I_{TM}=40A, $V_{DM}=V_{DRM(MAX)}$, I_G=0.1A, dI_G/dt=5A/µS	--	2	--	µs

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

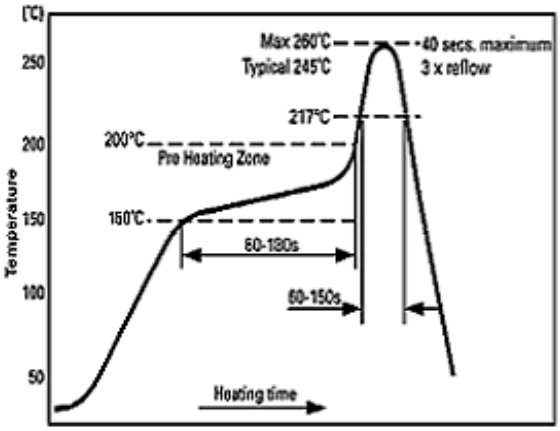
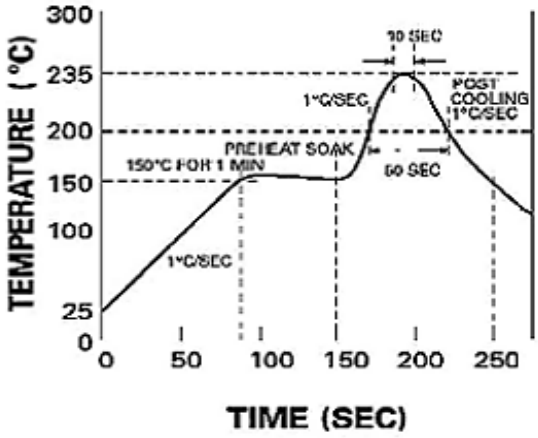


Figure 2

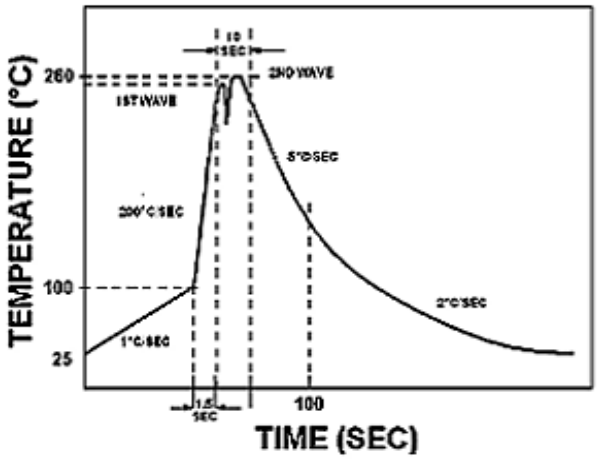


Reflow profiles in tabular form

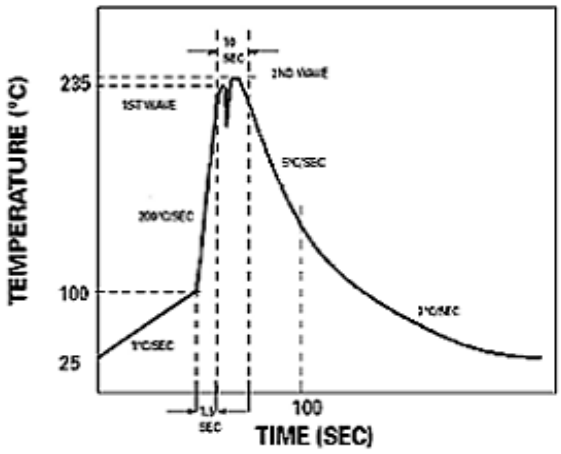
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Tim	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

TYPICAL CHARACTERISTICS CURVES

Fig 1: Maximum On-State Dissipation Ptot Versus Average On-State Current $I_{T(AV)}$

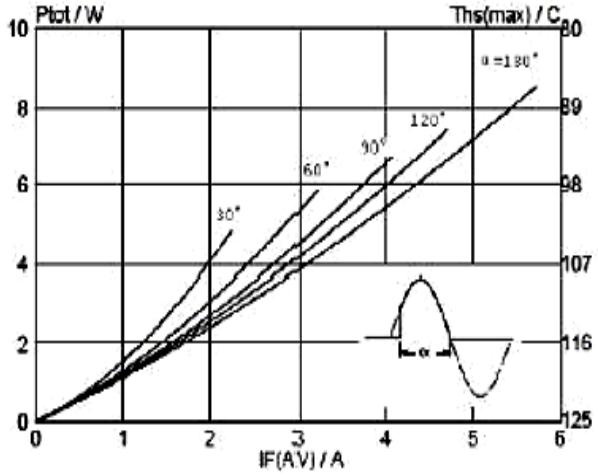


Fig 4: Typical and Maximum On-State Characteristics

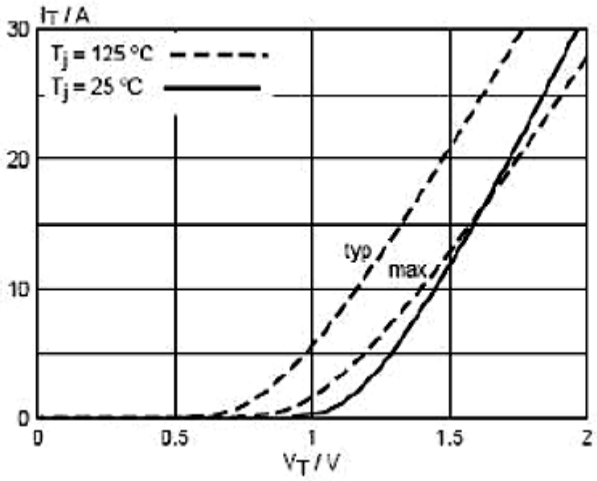
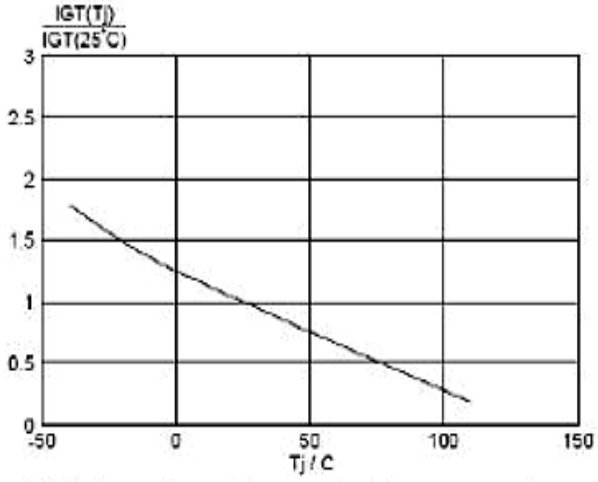
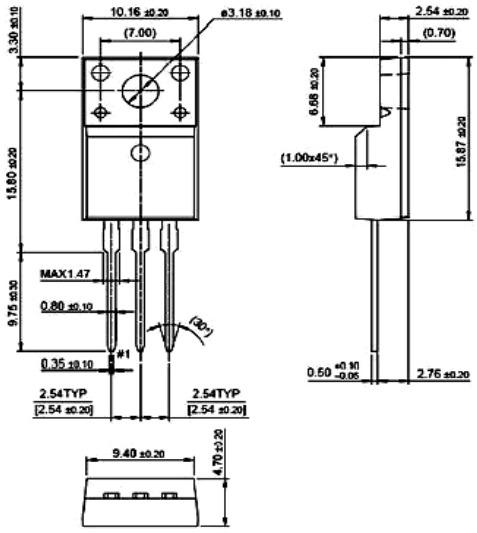


Fig 3: Normalized gate trigger current $I_{GT(Tj)}$ / $I_{GT}(25°C)$, Versus Junction Temperature T_j



Package Details

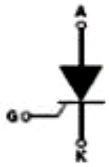
TO-220FP Fully Isolated



All Dimensions are in mm

Pin Configuration

1. Cathode
2. Anode
3. Gate



BT258X
Rev01_ 04102022E

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers.The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the Coil's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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