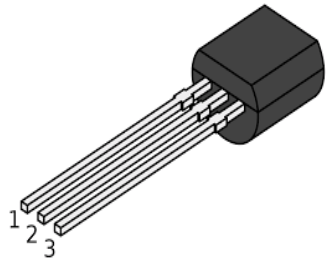


## N-CHANNEL POWER MOSFET

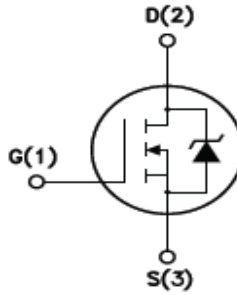
**CDB1N45**

**TO-92**

**Plastic Package**



1. Gate
2. Drain
3. Source



### Features

- 1) 100% Avalanche Tested
- 2) Typical  $R_{DS(on)} = 4.1\Omega$
- 3) Extremely High  $dv/dt$  Capability
- 4) Gate Charge Minimized

### Applications

- 1) Switch Mode Power Supplies (SMPS)
- 2) Low Power, Low Cost CFL (Compact Fluorescent Lamps)
- 3) Low Power Battery Chargers

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Drain - Source Voltage ( $V_{GS}=0$ )	$V_{DS}$	450	V
Drain - Gate Voltage ( $R_{GS}=20k\Omega$ )	$V_{DGR}$	450	V
Gate - Source Voltage	$V_{GS}$	$\pm 30$	V
Continuous Drain Current at $T_C = 25^\circ C$	$I_D$	0.5	A
Continuous Drain Current at $T_C = 100^\circ C$	$I_D$	0.315	A
Pulsed Drain Current	$* I_{DM}$	2	A
Total Power Dissipation at $T_C = 25^\circ C$	$P_{TOT}$	3.1	W
Derating Factor		0.025	W/ $^\circ C$
Peak Diode Recovery Voltage Slope	$dv/dt^{(1)}$	3	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ C$

\* Pulse Width Limited by Safe Operating Area

Note 1. -  $I_{SD} \leq 0.5A$ ,  $di/dt \leq 100A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{jmax}$

## ELECTRICAL CHARACTERISTICS ( $T_c = 25^\circ\text{C}$ Unless otherwise Specified)

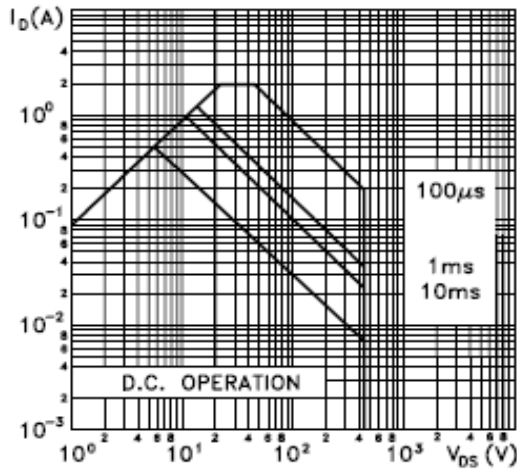
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
ON / OFF						
Drain - Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250μA	450			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = Max Rating, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> =Max Rating, V <sub>GS</sub> =0V, T <sub>J</sub> = 125°C			50	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±30V			±100	nA
Gate - Threshold Voltage	V <sub>GS (th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.3	3	3.7	V
Static Drain - Source On -State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.5A		4.1	4.5	Ω
Dynamic Characteristics						
Forward Transconductance	gfs <sup>(1)</sup>	V <sub>DS</sub> >I <sub>D(ON)</sub> X R <sub>DS(ON)MAX</sub> , I <sub>D</sub> =0.5A		1.1		S
Input Capacitance	Ciss	V <sub>DS</sub> = 25V V <sub>GS</sub> = 0 f =1.0 MHz		160		pF
Output Capacitance	Coss			27.5		
Reverse Transfer Capacitance	Crss			4.7		
Switching Characteristics						
Total Gate Charge	Qg	V <sub>DS</sub> = 360V, I <sub>D</sub> = 1.5A, V <sub>GS</sub> = 10V, R <sub>G</sub> =4.7Ω		7	10	nC
Gate - Source Charge	Qgs			1.3		
Gate - Drain Charge	Qgd			3.2		
Turn-on Delay Time	td(on)	V <sub>DD</sub> =225V, I <sub>D</sub> =0.5A, V <sub>GS</sub> =10V, R <sub>G</sub> =4.7Ω, (Resistive Load, See Fig.3)		6.7		ns
Rise Time	tr			4		
Off-Voltage Rise Time	t <sub>r(Voff)</sub>	V <sub>DD</sub> =360V, I <sub>D</sub> =1.5A, V <sub>GS</sub> =10V, R <sub>G</sub> =4.7Ω, (Inductive Load, See Fig.5)		8.5		ns
Fall Time	tf			12		
Cross-over Time	tc			18		
Source-Drain Diode Characteristics						
Source - Drain Current	I <sub>SD</sub>				1.5	A
Source - Drain Current (pulsed)	I <sub>SDM</sub> <sup>(2)</sup>				6	A
Forward On Voltage	V <sub>SD</sub> <sup>(1)</sup>	V <sub>GS</sub> = 0, I <sub>SD</sub> = 1.5A			1.6	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>DD</sub> = 100V, I <sub>SD</sub> = 1.5A, di/dt = 100A/μs, T <sub>J</sub> =150°C, (see test circuit, Fig.5)		225		ns
Reverse Recovery Charge	Q <sub>rr</sub>			530		nC
Reverse Recovery Current	I <sub>RRM</sub>			4.7		A

### Notes :

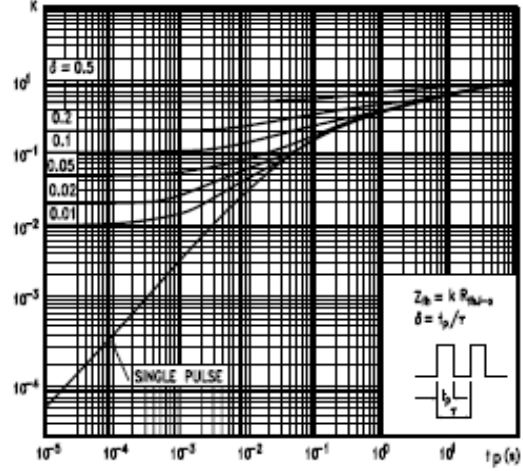
- 1) Pulse Duration =  $300\mu\text{s}$ , Duty Cycle = 1.5%
- 2) Pulse Width Limited by Safe Operating Area

## TYPICAL CHARACTERISTICS CURVES

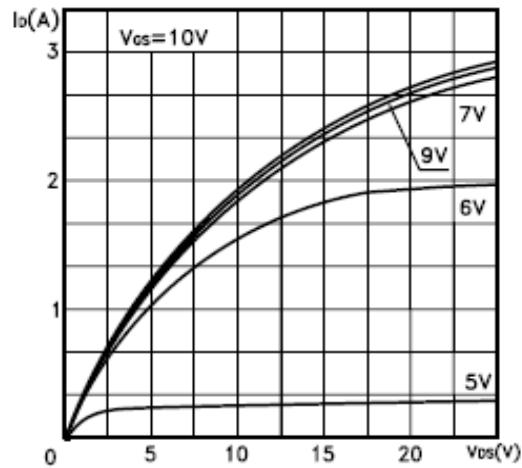
**Safe Operating Area**



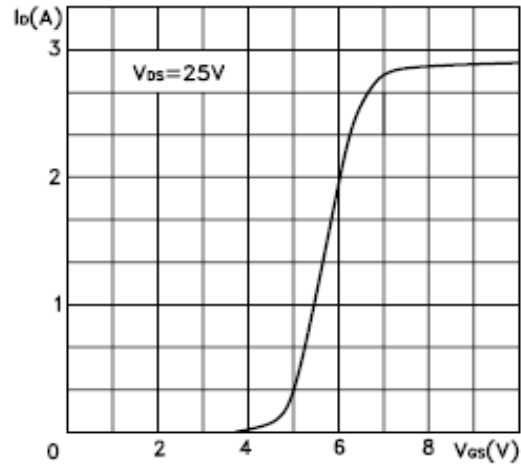
**Thermal Impedance**



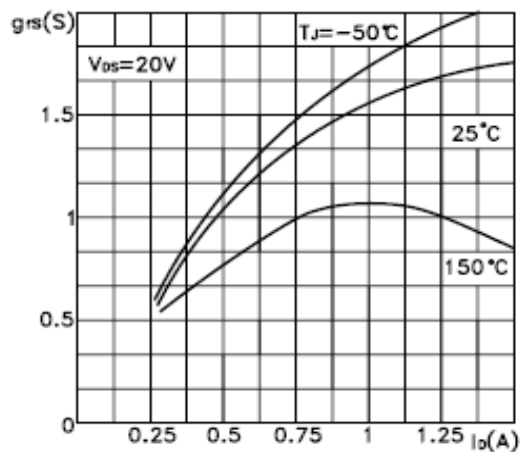
**Output Characteristics**



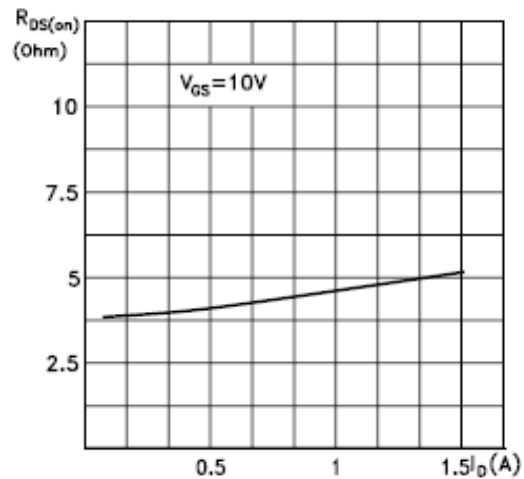
**Transfer Characteristics**



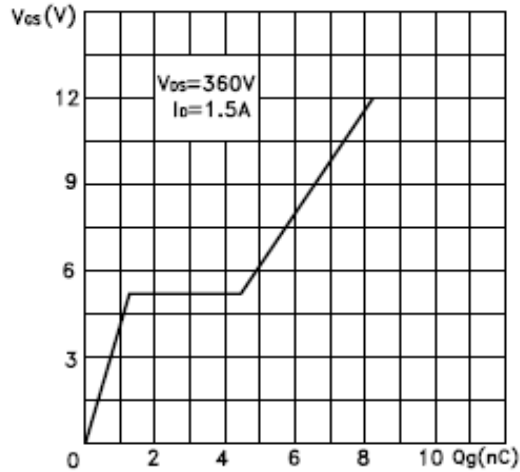
**Transconductance**



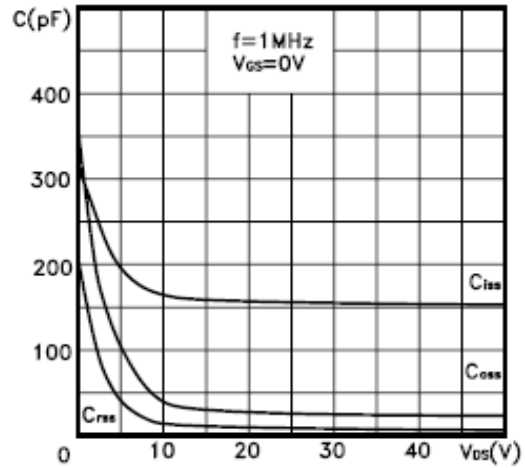
**Static Drain-source On Resistance**



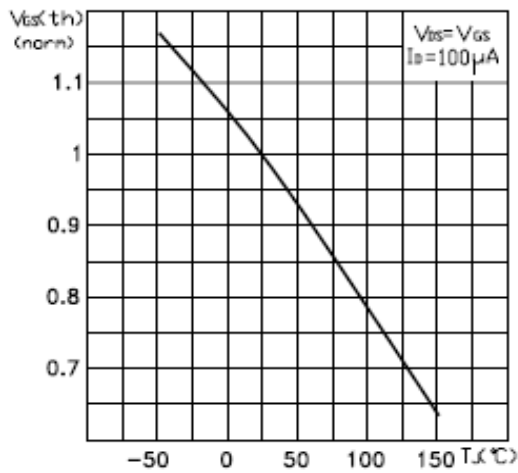
**Gate Charge vs Gate-source Voltage**



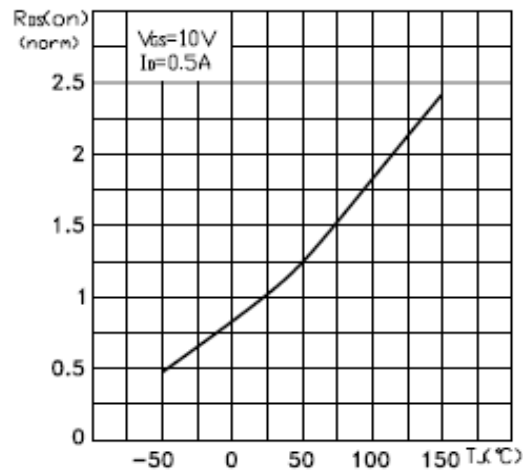
**Capacitance Variations**



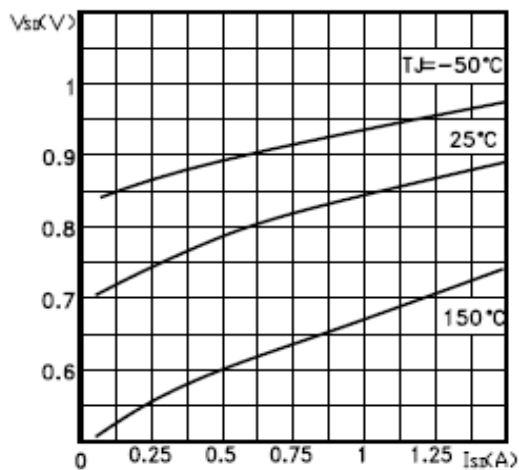
**Normalized Gate Threshold Voltage vs Temp.**



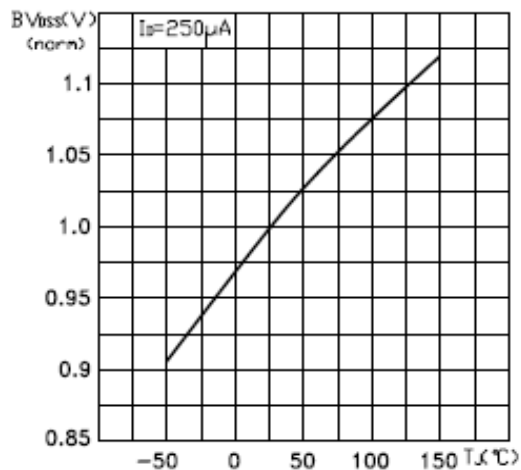
**Normalized On Resistance vs Temperature**



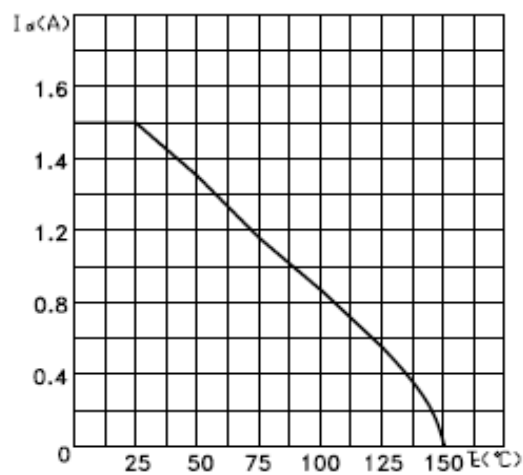
**Source-drain Diode Forward Characteristics**



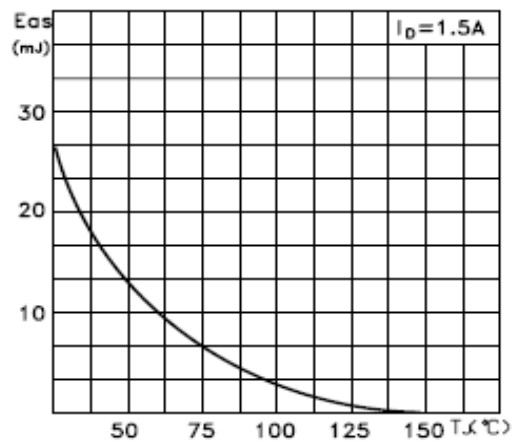
**Normalized BVDSS vs Temperature**



**Max Id Current vs Tc**



**Maximum Avalanche Energy vs Temperature**



## TEST CIRCUITS AND WAVEFORMS

Fig. 1: Unclamped Inductive Load Test Circuit

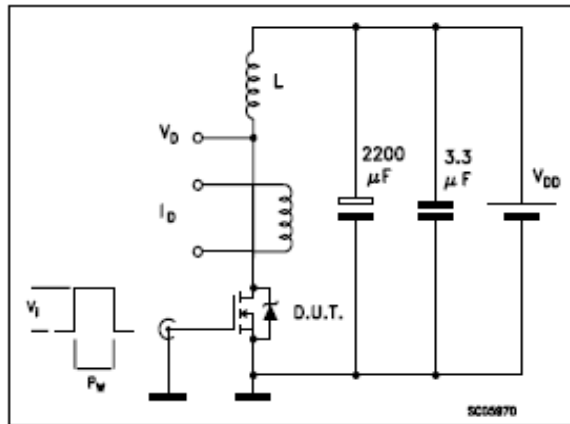


Fig. 2: Unclamped Inductive Waveform

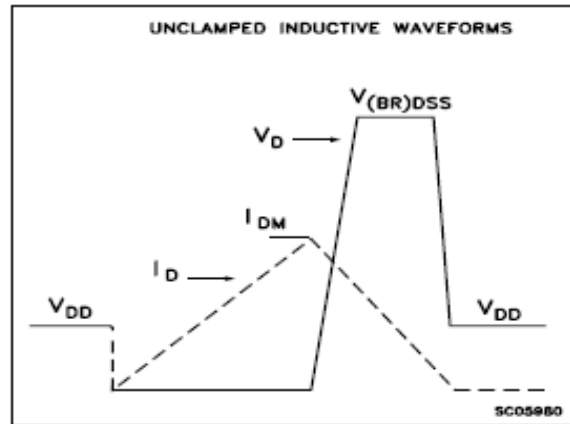


Fig. 3: Switching Times Test Circuit For Resistive Load

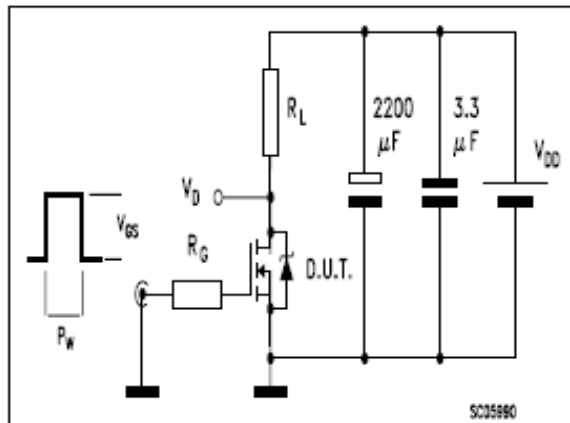


Fig. 4: Gate Charge test Circuit

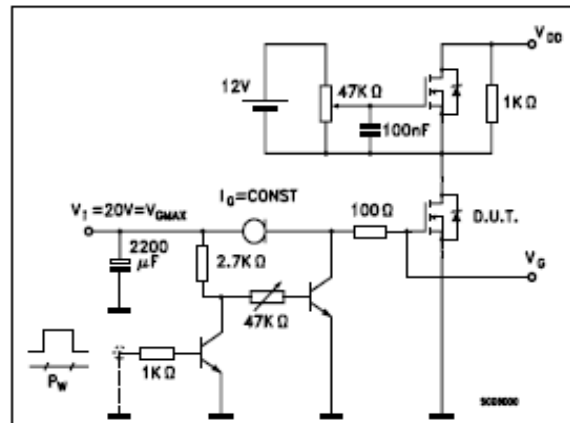
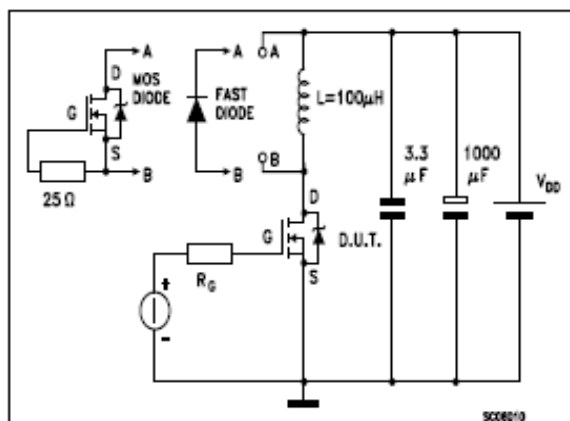
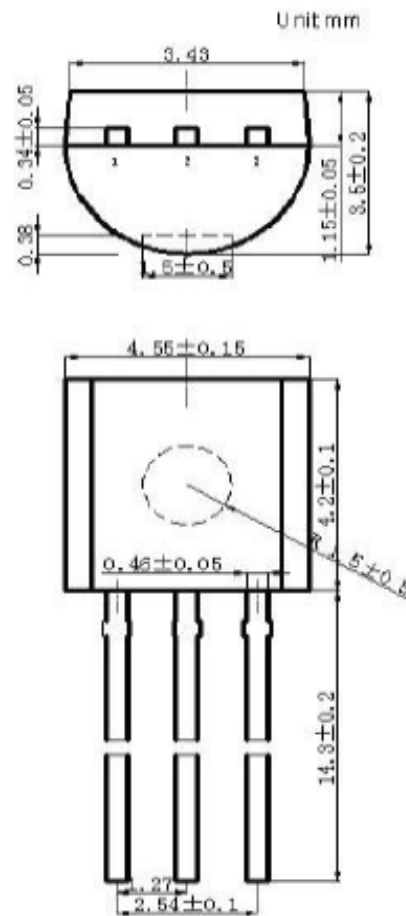


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-92 PACKAGE OUTLINE AND DIMENSIONS



1. Gate
2. Drain
3. Source



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C-120 Naraina Industrial Area, New Delhi 110 028, India.

Telephone + 91-11-2579 6150, 4141 1112 Fax + 91-11-2579 5290, 4141 1119

e-mail [sales@cdil.com](mailto:sales@cdil.com) [www.cdil.com](http://www.cdil.com)

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