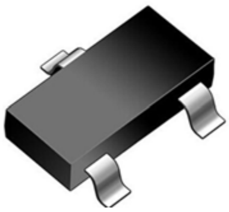
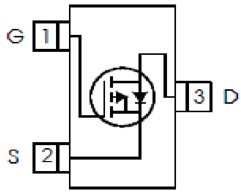
P Channel Power MOSFET

CLML6401

SOT-23
Surface Mount
Plastic Package





Features

1) Ultra Low On-Resistance
2) P-Channel MOSFET
3) SOT-23 Footprint
4) Low Profile (<1.1mm)
5) Available in Tape and Reel
6) Fast Switching
7) 1.8V Gate Rated
8) Lead-Free
9) RoHS Compliant, Halogen-Free

Description

These P-Channel MOSFET are sutilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in battery and load management.
A thermally enhanced large pad leadframe has been incorporated into the standard SOT-23 package to produce a Power MOSFET with the industry's smallest footprint.
This package, dubbed the SOT-23, is ideal for applications where printed circuit board space is at a premium.
The low profile(<1.1mm) of the Micro3 allows it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.
The thermal resistance and power dissipation are the best available.

Absolute Maximum Ratings

DESCRIPTION		SYMBOL	VALUE (Max)	UNIT
Drain- Source Voltage		V_{DS}	-12	V
Continuous Drain Current, VGS @ -4.5V ID @ TA = 25°C		I_D	-4.3	A
Continuous Drain Current, VGS @ -4.5V ID @ TA= 70°C		I_D	-3.4	
Pulsed Drain Current (1)		I_{DM}	-34	
Power Dissipation	PD @TA = 25°C	P_D	1.3	W
Power Dissipation	PD @TA = 70°C	P_D	0.8	
Linear Derating Factor			0.01	W/°C
Single Pulse Avalanche Energy(4)		E_{AS}	33	mJ
Gate-to-Source Voltage		V_{GS}	±8.0	V
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to + 150	°C

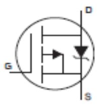
Thermal Characteristics

DESCRIPTION		SYMBOL	VALUE		UNIT
Maximum Junction-to-Ambient(3)		$R_{\theta JA}$	75 (Typ.)	100 (Max)	°C/W

ELECTRICAL CHARACTERISTICS (TA=25□ unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-12	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.007	—	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.050	Ω	V_{GS} = -4.5V, I_D = -4.3A ②
		—	—	0.085		V_{GS} = -2.5V, I_D = -2.5A ②
		—	—	0.125		V_{GS} = -1.8V, I_D = -2.0A ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.40	-0.55	-0.95	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	8.6	—	—	S	V_{DS} = -10V, I_D = -4.3A
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	µA	V_{DS} = -12V, V_{GS} = 0V
		—	—	-25		V_{DS} = -9.6V, V_{GS} = 0V, T_J = 55°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -8.0V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 8.0V
Q_g	Total Gate Charge	—	10	15	nC	I_D = -4.3A
Q_{gs}	Gate-to-Source Charge	—	1.4	2.1		V_{DS} = -10V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.6	3.9		V_{GS} = -5.0V②
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD} = -6.0V
t_r	Rise Time	—	32	—		I_D = -1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	250	—		R_D = 6.0Ω
t_f	Fall Time	—	210	—		R_G = 89Ω ②
C_{iss}	Input Capacitance	—	830	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	180	—		V_{DS} = -10V
C_{rss}	Reverse Transfer Capacitance	—	125	—		f = 1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-34		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	T_J = 25°C, I_S = -1.3A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	—	22	33	ns	T_J = 25°C, I_F = -1.3A
Q_{rr}	Reverse RecoveryCharge	—	8.0	12	nC	di/dt = -100A/µs ②

Notes
(1) Repetitive rating; pulse width limited by max. junction temperature.
(2) Pulse width ≤ 300µs; duty cycle ≤ 2%.
(3) Surface mounted on 1" square single layer 1oz copper FR4 board.steady state.
(4) Starting TJ = 25°C, L = 3.5mH RG = 25Ω, IAS = -4.3A.

TYPICAL CHARACTERISTICS CURVES

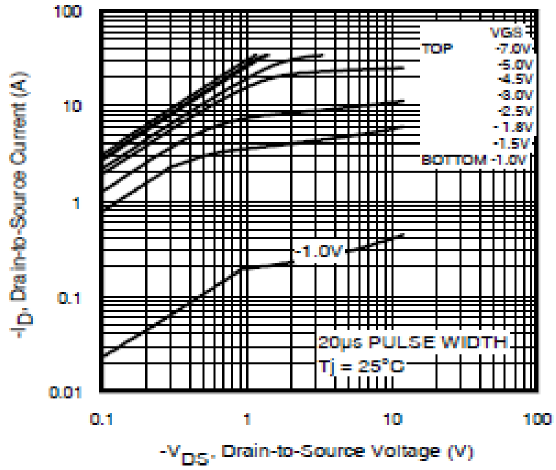


Fig 1. Typical Output Characteristics

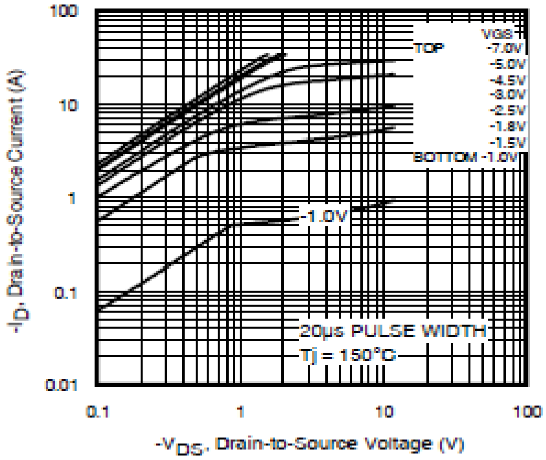


Fig 2. Typical Output Characteristics

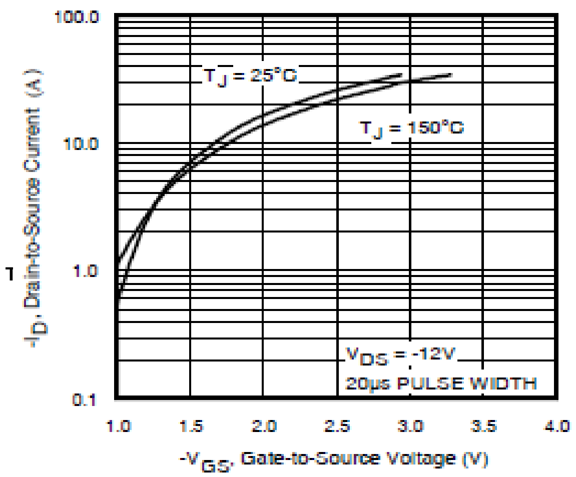


Fig 3. Typical Transfer Characteristics

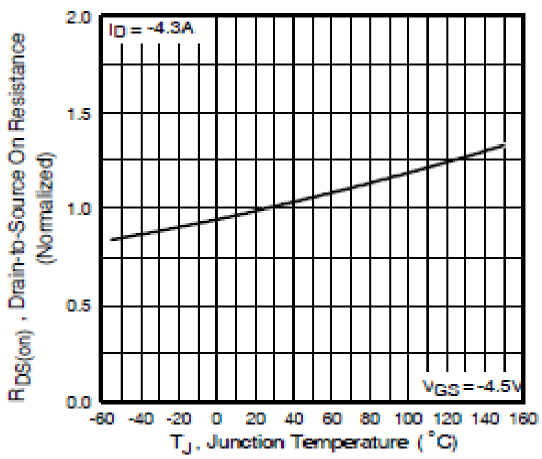


Fig 4. Normalized On-Resistance
Vs. Temperature

TYPICAL CHARACTERISTICS CURVES (Continued….)

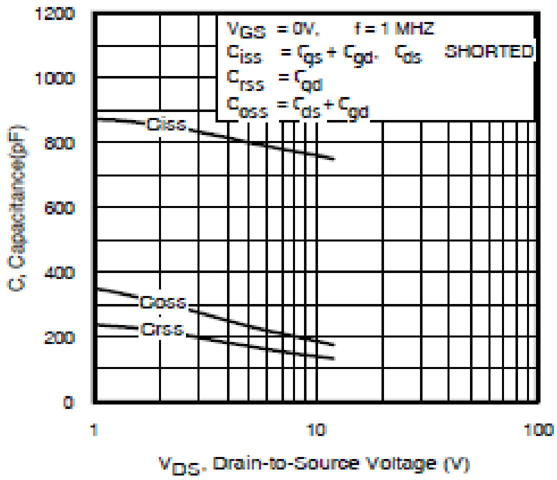


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

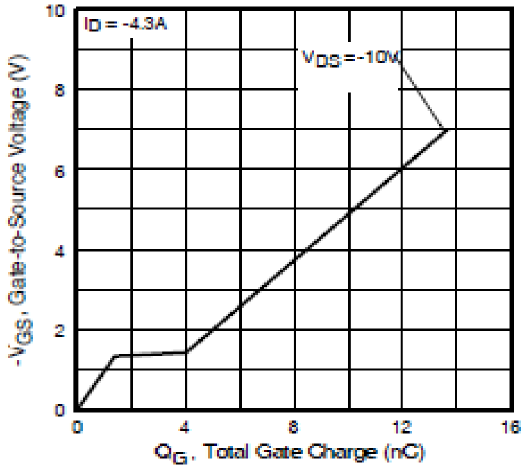


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

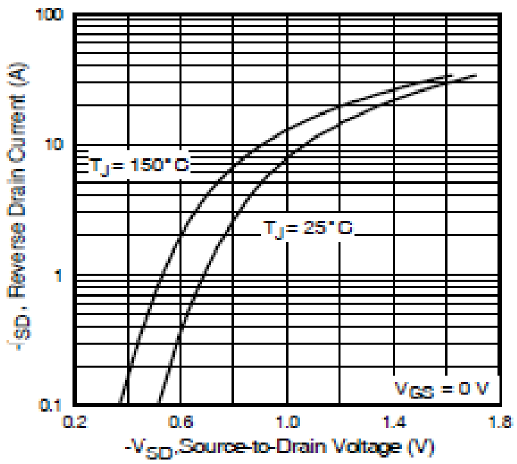


Fig 7. Typical Source-Drain Diode Forward Voltage

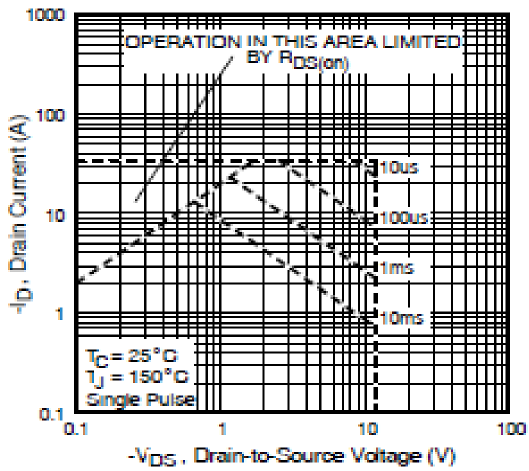


Fig 8. Maximum Safe Operating Area

TYPICAL CHARACTERISTICS CURVES (Continued….)

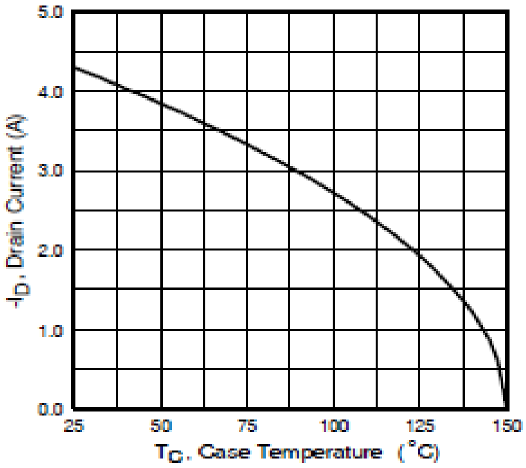


Fig 9. Maximum Drain Current Vs. Case Temperature

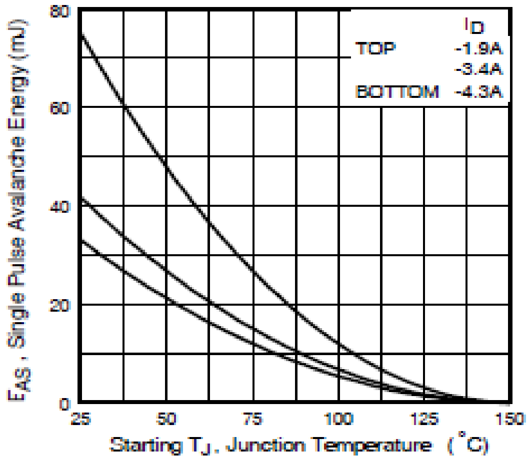


Fig 10. Maximum Avalanche Energy Vs. Drain Current

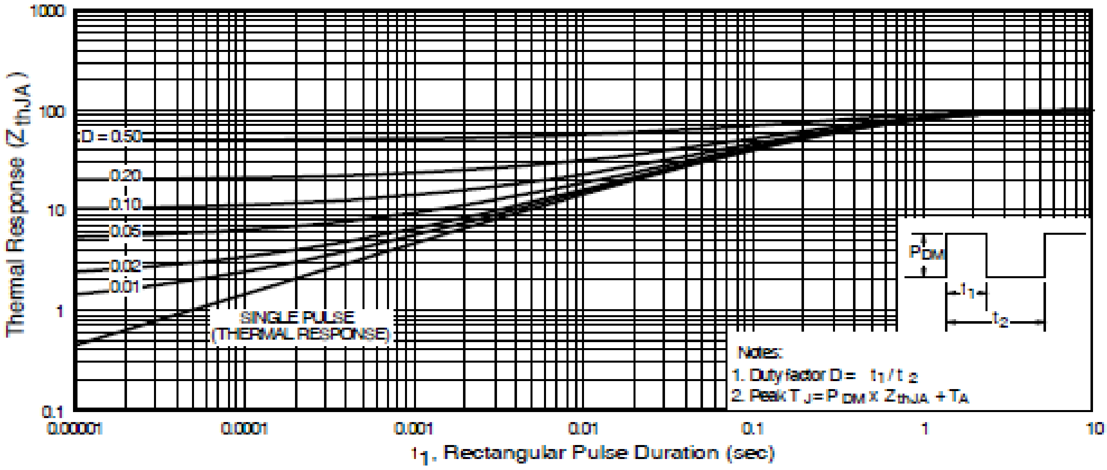


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS CURVES (Continued….)

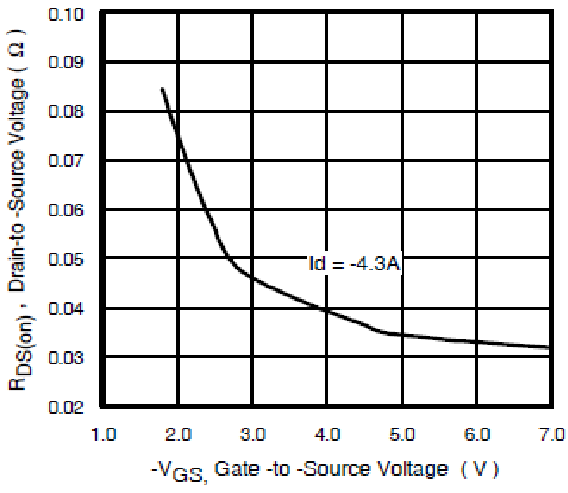


Fig 12. Typical On-Resistance Vs. Gate Voltage

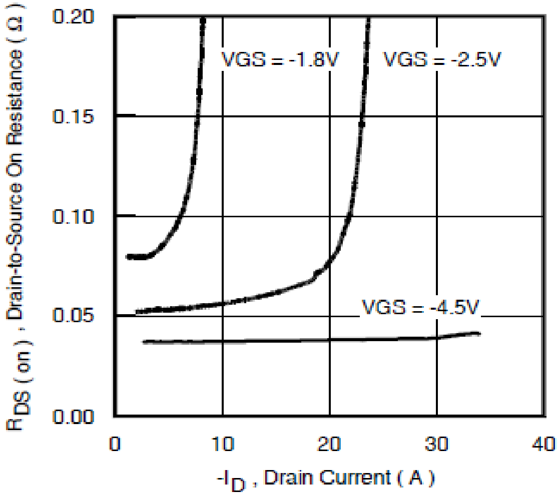


Fig 13. Typical On-Resistance Vs. Drain Current

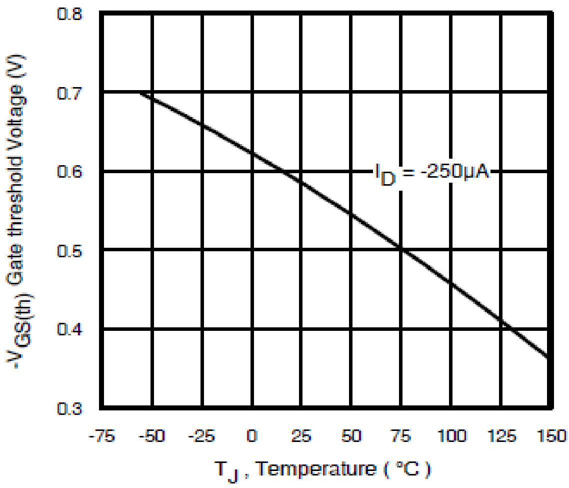
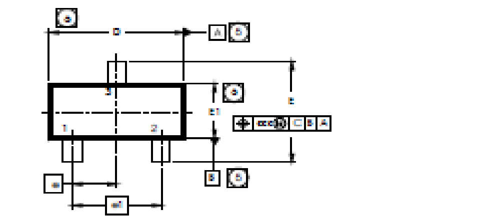


Fig 14. Typical Threshold Voltage Vs. Junction Temperature

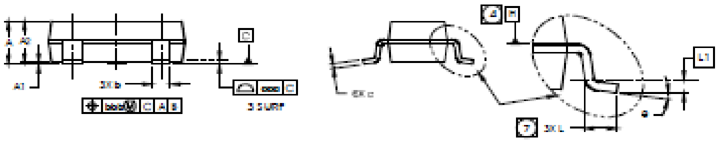
Package Details

SOT-23 Lead-Free Package Outline

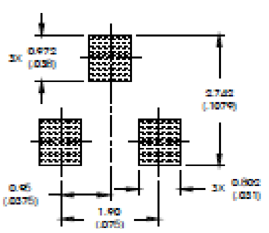
Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.89	1.12	.036	.044
A1	0.01	0.10	.0004	.0039
A2	0.88	1.02	.035	.040
b	0.30	0.50	.0119	.0196
c	0.08	0.20	.0032	.0078
D	2.80	3.04	.111	.119
E	2.10	2.64	.083	.103
E1	1.20	1.40	.048	.055
e	0.95 BSC		.0375 BSC	
e1	1.90 BSC		.075 BSC	
L	0.40	0.60	.0158	.0236
L1	0.25 BSC		.0118 BSC	
θ	0°	8°	0°	8°
aaa	0.10		.004	
bbb	0.20		.008	
ccc	0.15		.006	



RECOMMENDED FOOTPRINT



NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE MOLD PARTING LINE.
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-236AB.

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.

2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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