Synchronous Rectifier

Package- SOP8
C6501

General Description

C6501 is a smart secondary-side switch IC designed for isolated fly-back system. The IC emulate the behavior of Schottky diode rectifier for reduces power dissipation. C6501 works in DCM and QR operation modes. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in all operating modes. C6501 senses the build-in MOSFET drain-source voltage, and output ideal drive signal with less external components. It only provides high performance solution for 5V output voltage application.

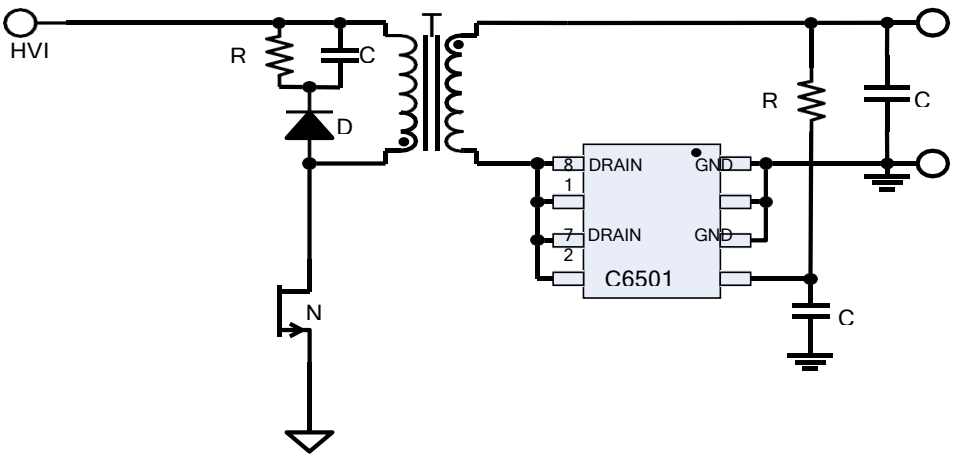
Features

1. Build-in 16mΩ 45V MOSFET
2. Low current consumption
3. Up to 70KHz operation frequency
4. 1.2-Ω Sink,3.0-Ω Source Gate-Drive Impedance
5. 50ns turn-off propagation delay
6. VCC range from 3V to 6V
7. VCC OVP Clamping
8. Cycle by Cycle MOT Check Circuit prevents multiple false trigger Gate pulses
9. DCM and QR operation
10. SOP8 Package

Applications

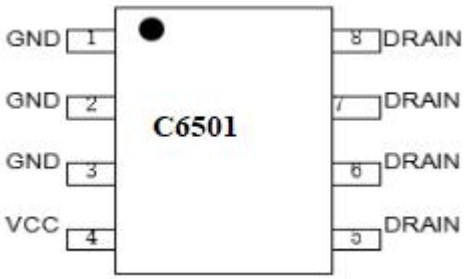
1. 5V AC-DC adaptors
2. Battery Powered systems.
3. Digital Cameras Charger

Simplified Application



PIN Configuration and Description

Pin Diagram



Pin No.	Pin Name	Function Description
1,2,3	GND	Power Ground Return for MOSFET Source
4	VCC	Inner Power Supply, Connect Capacitor to Ground
5,6,7,8	DRAIN	MOSFET Drain side

Ordering and Marking Information

Part Number	Package Description	Top Marking	Package Form
C3056FL	SOP8, Pb-free	C3056FL	SOP8

Absolute Maximum Ratings

Symbol	Description	Value	Units
DRAIN	MOSFET Drain	-1 to 45	V

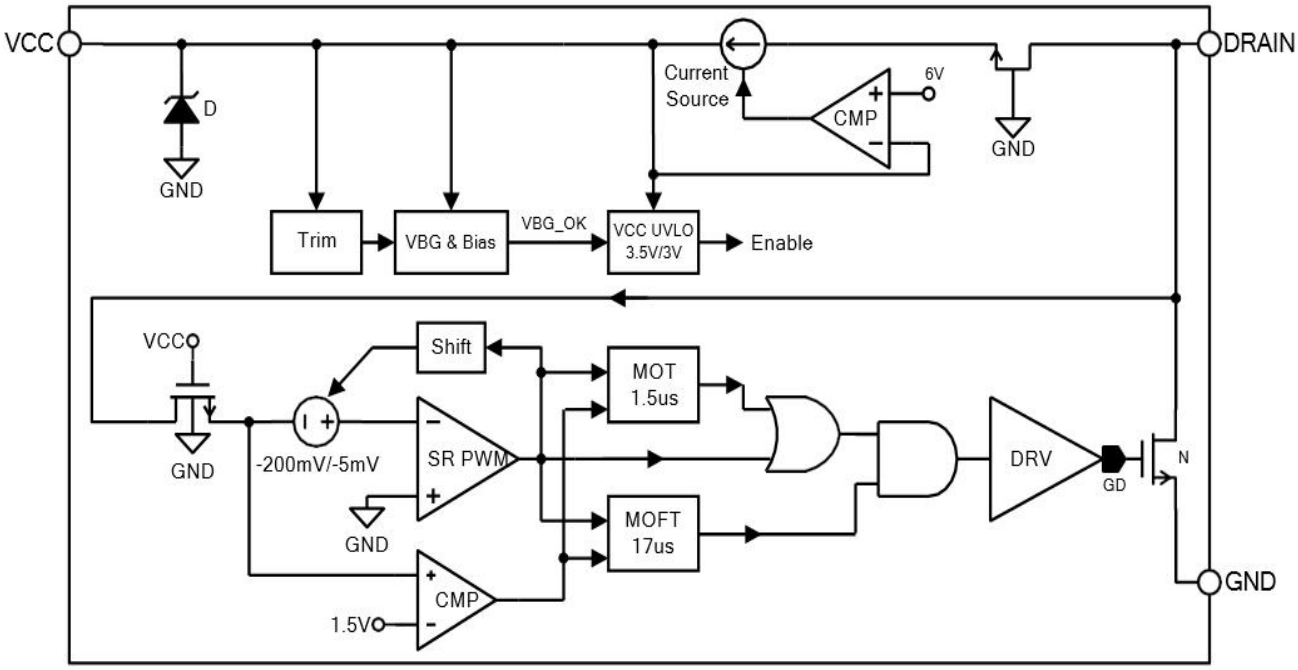
VCC	VCC Input Voltage	-0.3 to 7	V
T_J	Operating Junction Temperature	-40 to 125	℃
T_{stg}	Min/Max Storage Temperature	-55 to 150	℃
T_L	Lead Temperature (Soldering. 10secs)	260	℃

Note Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Description	Value	Units
VCC	VCC Supply Voltage	5	V
	VCC bypass Capacitor	>1	uF
Fsw	Switch Frequency	<70	KHz
DRAIN	MOSFET Drain Voltage	-0.6~40	V

Block Diagram:



Typical Application Diagram

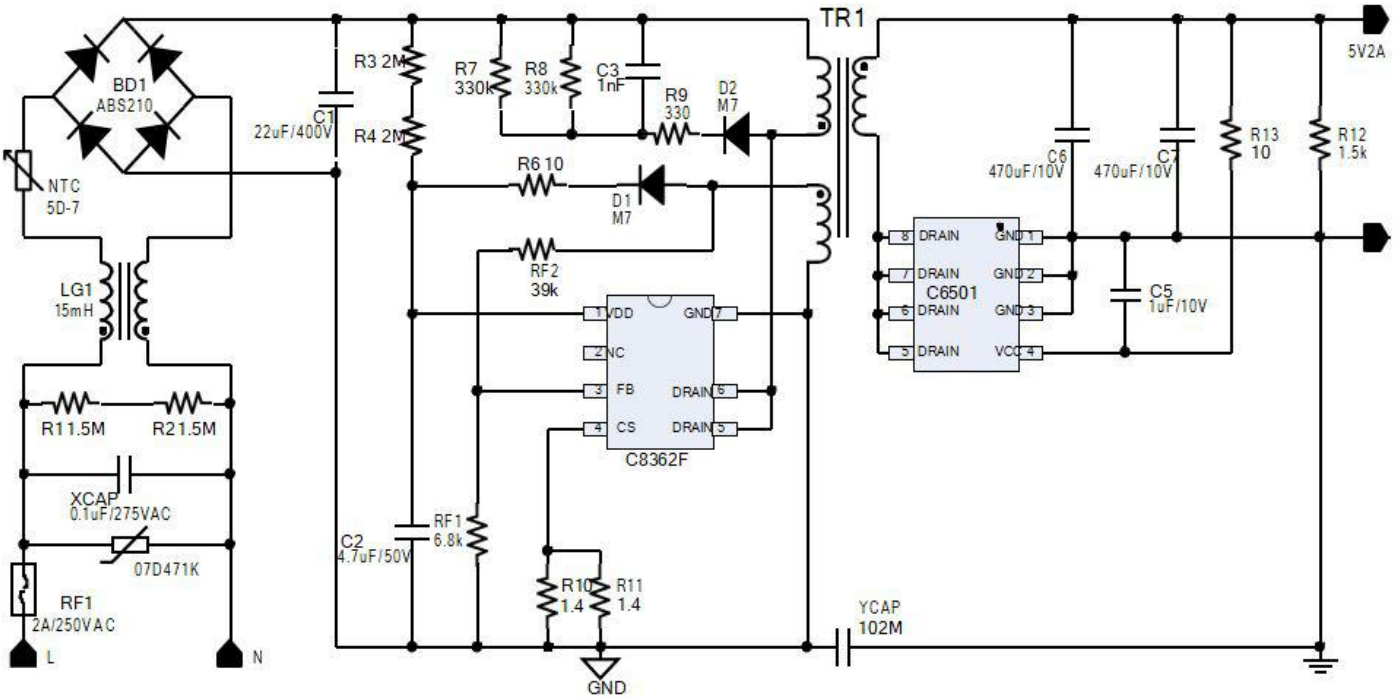
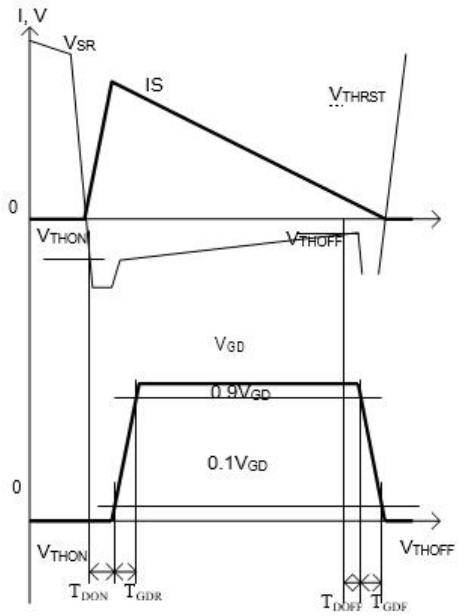


Figure 3. Schematic of Typical Application Circuit

Functional Description

C6501 detects the internal MOSFET drain-source voltage (VDS). When the drain voltage is lower than the turn-on threshold voltage (VTHON), it outputs a positive drive voltage after a turn-on delay time (TDON). The internal MOSFET will turn on and the current will transfer from the body diode into the internal MOSFET's channel, then lower conduction loss can be achieved. In the process of internal MOSFET channel current decreasing linearly toward zero, the drain-source voltage rises synchronically. When it rises over the turn off threshold voltage (VTHOFF), C6501 pulls down the internal MOSFET gate voltage to zero after a turn off delay time (TDOFF) as shown in figure below.



Typical Waveforms of C6501

Power Supply

The IC supply voltage is monitored by the under-lockout circuit. It is possible to turn off the IC by pulling VCC pin below the minimum turn off threshold voltage, without damaging the IC. To prevent noise problems, a bypass ceramic capacitor connected to VCC and GND should be placed as close as possible to IC. This pin is internally clamped at 6.3V.

UVLO Mode

The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage VCC_ON. During the time the IC remains in the UVLO state, the gate drive circuit is inactive, and the IC draws a quiescent current of ICC START. The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of VCC < VCC_OFF occurs.

Minimum Turn-On Time

When the controlled internal MOSFET gate is turned on, some ringing noise is generated. The minimum on time blanks the VTHOFF comparator, keeping the controlled internal MOSFET on for at least the minimum on time. If VTHOFF falls below the threshold before minimum on time expires, the internal MOSFET will keep on until the end of the minimum on time.

Drain Voltage Inner Sense

DRAIN pin is used to sense the internal MOSFET Drain voltage. This is a high voltage pin and care must be taken in properly routing the connection to the internal MOSFET drain side.

Normal Mode

The IC enters in normal operating mode once the UVLO voltage has been exceeded. When the IC enters Normal Mode from UVLO Mode, the GATE output is disabled (stays low) until VSR exceeds VTHRST to activate the gate. This ensures that the GATE output is not enabled in the middle of a switching cycle. This logic prevents any reverse currents across the device due to minimum on time function in the IC. The gate will continuously drive the SR internal MOSFET after this one-time activation. The Cycle by Cycle MOT protection circuit is enabled in Normal Mode.

MOT Protection Mode

If the secondary current conduction time is shorter than the MOT (Minimum On Time) setting, the next driver output is disabled. This function can avoid reverse current that occurs when the system works at very low duty-cycles or at very light/no load conditions and reduce system standby power consumption by disabling GATE outputs. The Cycle by Cycle MOT Check circuit is always activated under Normal Mode and MOT Protection Mode, so that the IC can automatically resume normal operation once the load increases to a level and the secondary current conduction time is longer than MOT.

Turn-on phase

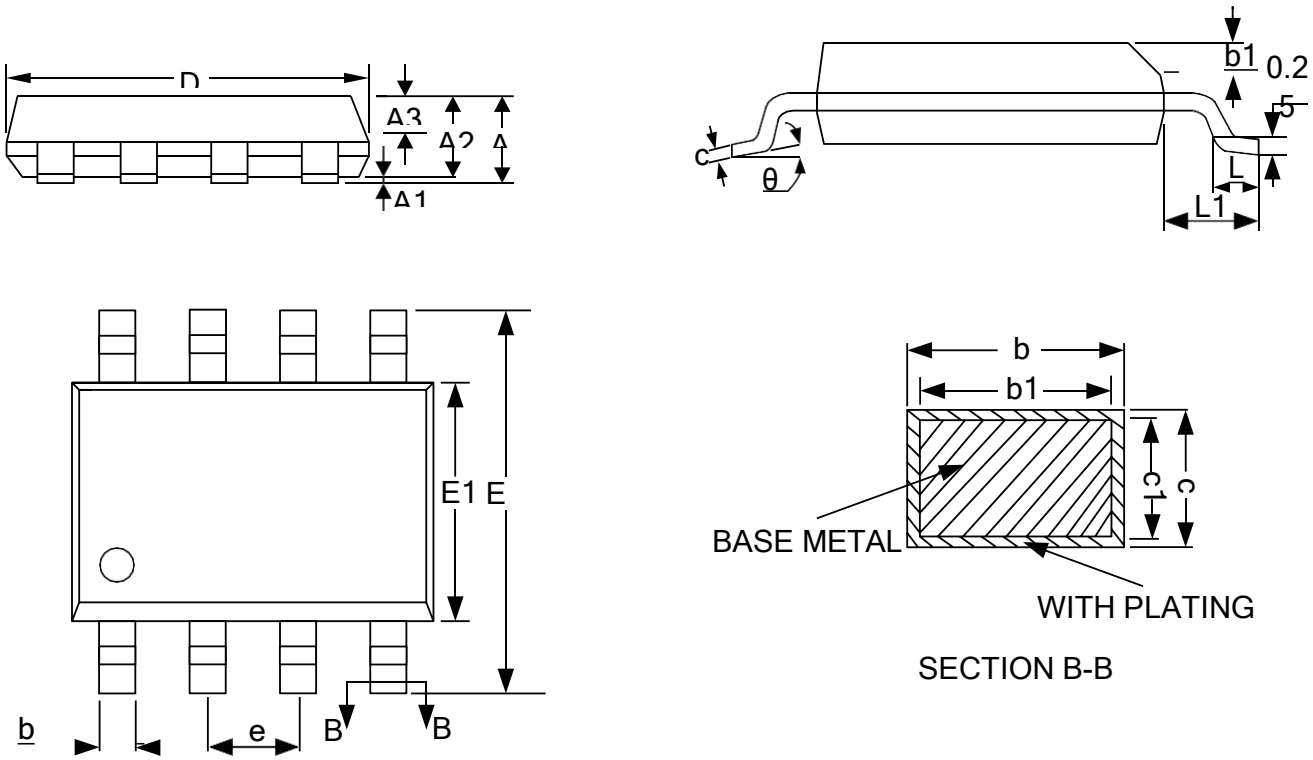
When the conduction phase of the SR internal MOSFET is initiated, current will start flowing through its body diode, generating a negative VDS voltage across it. The body diode has generally a much higher voltage drop than the one caused by the internal MOSFET on resistance and therefore will trigger the turn-on threshold VTHON. At that point, C6501 will drive the gate of internal MOSFET on, which will in turn cause the conduction voltage VDS to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off, hence, a Minimum On Time (MOT) blanking period is used that will maintain the power internal MOSFET on for a minimum amount of time. Once the SR internal MOSFET has been turned on, it will remain on until the rectified current will decay to the level where internal MOSFET VDS will cross the turn-off threshold VTHOFF. This will happen differently depending on the mode of operation. In DCM the current will cross the threshold with a relatively low dI/dt. Once the threshold is crossed, C6501 will turn off gate and the current will start flowing again through the body diode, causing the VDS voltage to jump negative. Depending on the amount of residual current, internal MOSFET VDS may trigger once again the turn on threshold. For this reason, VTHON is blanked for a certain amount of time (TBLANK) after VTHOFF has been triggered. The blanking time is internally set. As soon as internal MOSFET VDS crosses the positive threshold VTHRST, the blanking time is terminated, and IC is ready for next

conduction cycle.

Electrical Characteristics

VDD=16V, TA=25℃, unless otherwise noted.						
Symbol	**Description**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
VCC Section						
ICC	Quiescent Current			110	150	uA
V_{CC_ON}	VCC ON Voltage	VCC Going Up	3.4	3.5	3.6	V
V_{CC_OFF}	VCC OFF Voltgae	VCC Going Down	2.9	3	3.1	V
V_{CC_OVP}	VDD over voltage protection		6	6.3	6.6	V
SR Section						
MOT	Minimum ON Time			1.5	2	us
MOFT	Minimum OFF Time			17		us
V_{THON}	SR ON threshold	SR Voltage down		-200		mV
V_{THOFF}	SR OFF threshold	SR Voltage up		-5		mV
V_{THRST}	SR Reset threshold	SR Voltage up		1.5		V
VD Section						
ID	VD Current Source	VD=30V，VCC=0V		15		mA
Inner GD Section						
Rgd_up	Gate Pull up Resistance			3		Ω
Rgd_down	Gate Pull down Resistance			12		Ω
$F_{_MAX}$	Maximum frequency		70			KHz
T_{DON}	Turn On Delay Time	SR down to GD=4V		85		ns
T_{DOFF}	Turn OFF Delay Time	SR up to GD=1V		45		ns
T_{GDR}	Turn On Rising Time	From 1V to 4V, CL=6.3nF		70		ns
T_{GDF}	Turn Off Falling Time	From 4V to 1V, CL=6.3nF		40		ns
MOS Section						
RDSON	Static drain to source on resistance	VCC=5V		16		mΩ

Package Information (Unit:mm)



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SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	—	—	1.75	D	4.70	4.90	5.10
A1	0.05	—	0.15	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	—	0.48	h	0.25	—	0.50
b1	0.38	0.41	0.43	L	0.50	—	0.80
c	0.21	—	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	—	8°

Recommended Product Storage Environment for Diode and Transistors

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature **5 °C to 30 °C**
- Humidity between **40 to 70 %RH**
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years, the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start. For this the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤ 30 °C / 85% RH
2	1 Year	≤ 30 °C / 60% RH
2a	4 Weeks	≤ 30 °C / 60% RH
3	168 Hours	≤ 30 °C / 60% RH
4	72 Hours	≤ 30 °C / 60% RH
5	48 Hours	≤ 30 °C / 60% RH
5a	24 Hours	≤ 30 °C / 60% RH
6	Time on Label(TOL)	≤ 30 °C / 60% RH

Figure 1 Floor Life according to JEDEC MSL Level

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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