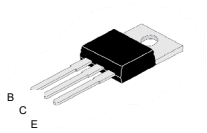
MEDIUM POWER COMPLEMENTRY DARLINGTON SILICON TRANSISTORS

PNP **NPN**
2N6040 **2N6043**
2N6041 **2N6044**
2N6042 **2N6045**



TO-220

T0-220 Leaded
Plastic Package
RoHS compliant

APPLICATIONS:

Designed for general purpose amplifier and low-speed switching applications

ABSOLUTE MAXIMUM RATINGS (T_a = 25 ^{O}C)

PARAMETER	SYMBOL	VALUE			UNIT
		2N6040	2N6041	2N6042	
		2N6043	2N6044	2N6045	
Collector-Emitter Voltage	V_{CEO}	60	80	100	V
Collector-Base Voltage	V_{CBO}	60	80	100	V
Emitter-Base Voltage	V_{EBO}	5			V
Collector Current-Continuous	I_C	8.0			A
Collector Current-Peak	I_{CM}	16			
Base Current	I_B	120			mA
Total Power Dissipation @ T_C=25°C	P_D	75			W
Derate above 25°C		0.6			W/°C
Operating and Storage Junction Temperature Range	T_J , T_{STG}	-65 to +150			°C

THERMAL RESISTANCE

Junction to Case	$R_{\theta jc}$	1.67	^{O}C/W

ELECTRICAL CHARACTERISTICS (Tc = 25℃ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage [1] 2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	$V_{CEO(sus)}$	I_C = 30mA , I_B =0	60 80 100	--	--	V
Collector Cutoff Current 2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	I_{CEO}	V_{CE}=30V, I_B=0 V_{CE}=40V, I_B=0 V_{CE}=50V, I_B=0	--	--	0.5 0.5 0.5	mA
Collector Cutoff Current 2N6040, 2N6043 2N6041, 2N6044 2N6042, 2N6045	I_{CBO}	V_{CB}=60V, I_E=0V V_{CB}=80V, I_E=0 V_{CB}=100V, I_E=0	--	--	0.5 0.5 0.5	mA
Emitter Cutoff Current	I_{EBO}	V_{EB}=5.0V, I_C=0	--	--	2.0	mA
ON CHARACTERISTICS [1]						
DC Current Gain 2N6040,41,43,44 2N6042,45 All types	h_{FE}	I_C=4.0 A, V_{CE}=4.0V I_C=3.0 A, V_{CE}=4.0V I_C=8.0 A, V_{CE}=4.0V	1000 1000 100	--	20000 20000	
Collector-Emitter Sustaining Voltage [1] 2N6040,41,43,44 2N6042,45 All types	$V_{CE(sat)}$	I_C=4.0 A, I_B=16 mA I_C=3.0 A, I_B=12 mA I_C=8.0 A, I_B=80 mA	--	--	2.0 2.0 4.0	V
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=8.0 A, I_B=80 mA	--	--	4.5	V

Note:

1. Pulse Test width = 300 μs , Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS CURVES

Fig 1: Power Derating

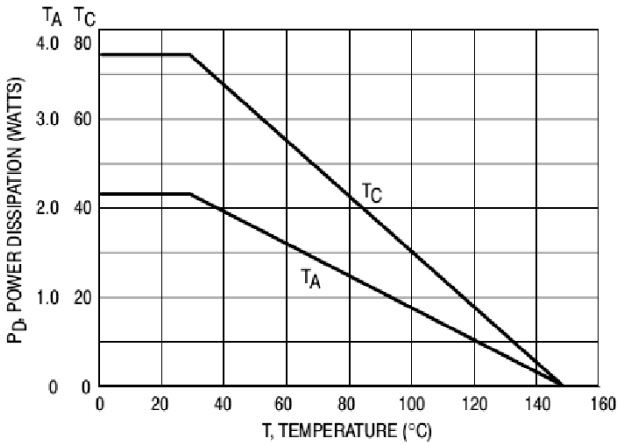


Fig 2: Power Derating

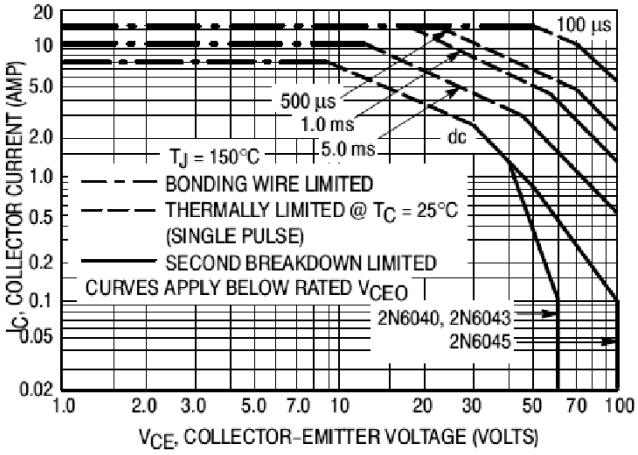


Fig 3:Thermal Response

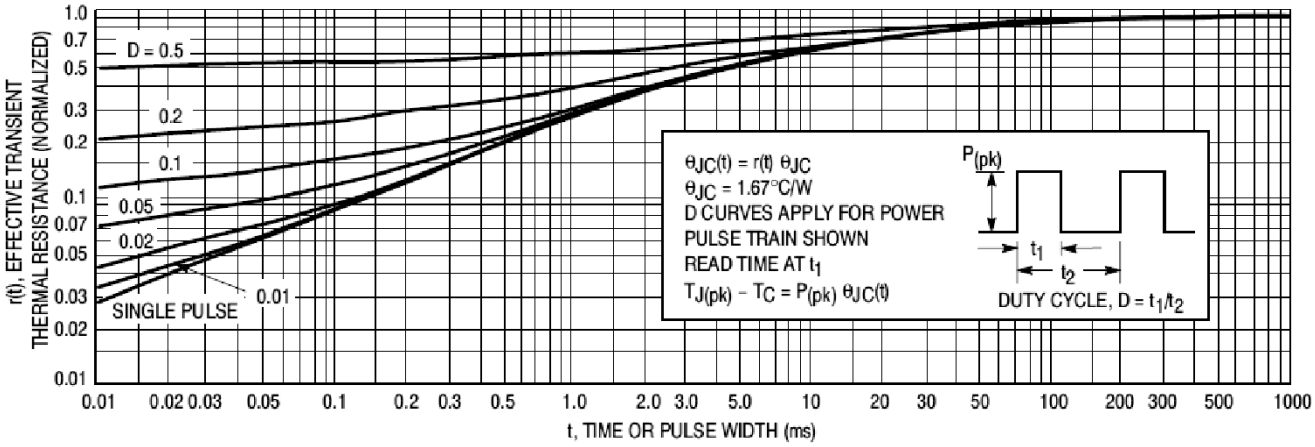


Fig 4: Switching Times Equivalent Circuit

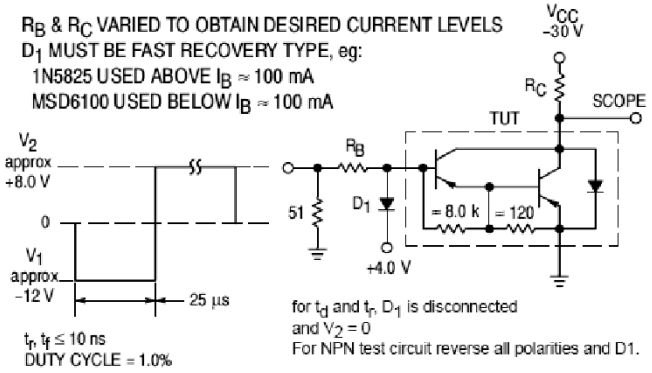
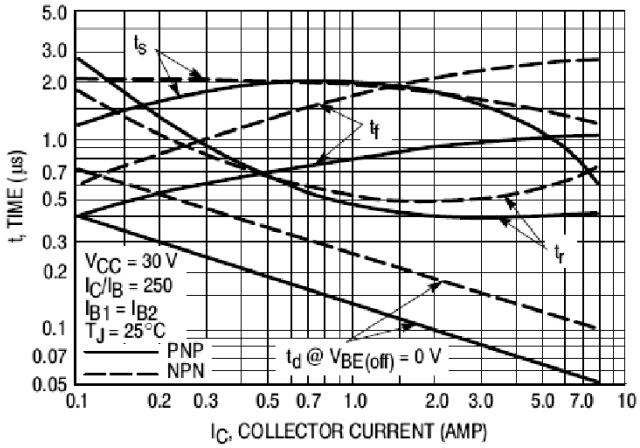


Fig 5: Switching Times



TYPICAL CHARACTERISTICS CURVES

Fig 6: Small–Signal Current Gain

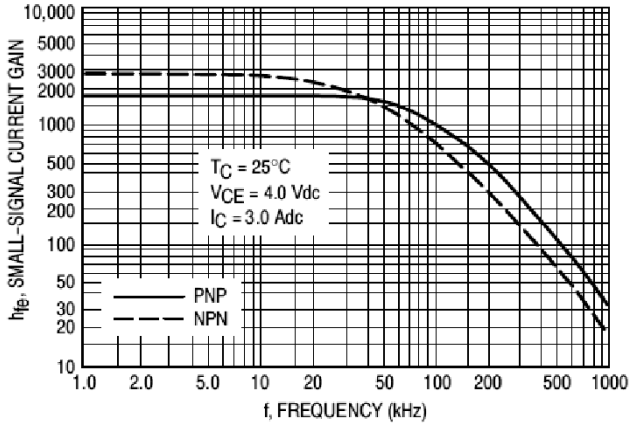


Fig 7 : Capacitance

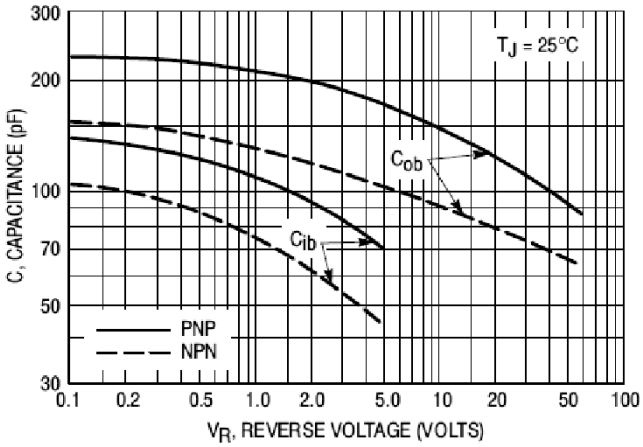
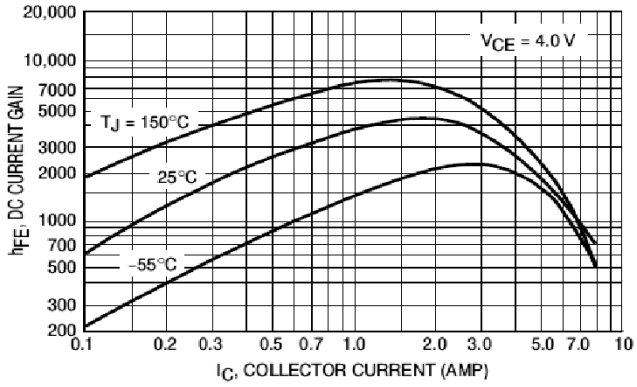
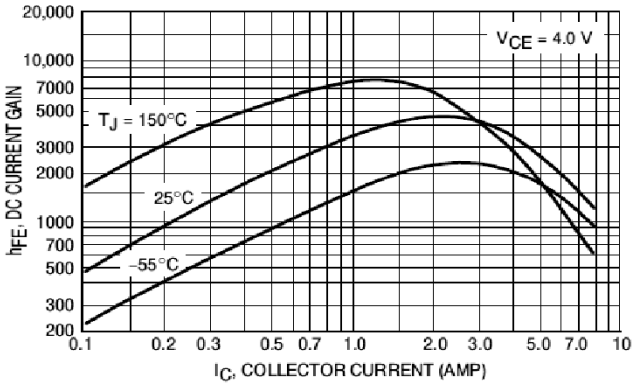


Fig 8: DC Current Gain

PNP
2N6040, 2N6042

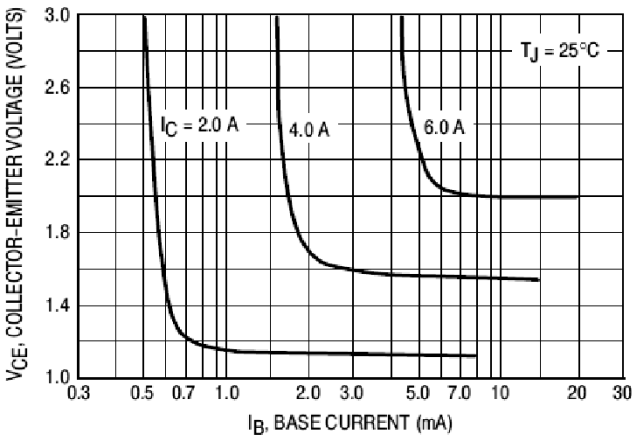


NPN
2N6043, 2N6045



TYPICAL CHARACTERISTICS CURVES

Fig 9: Collector Saturation Region



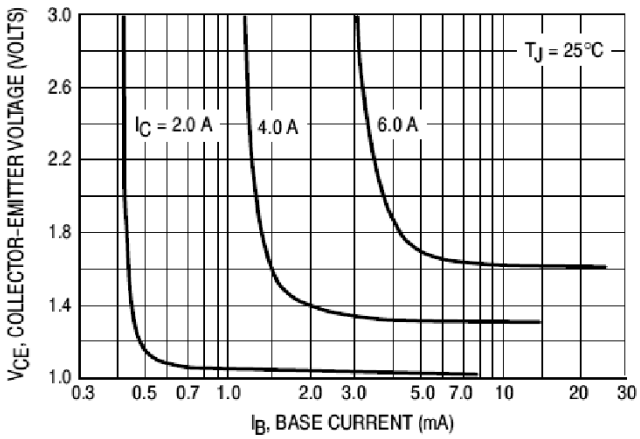
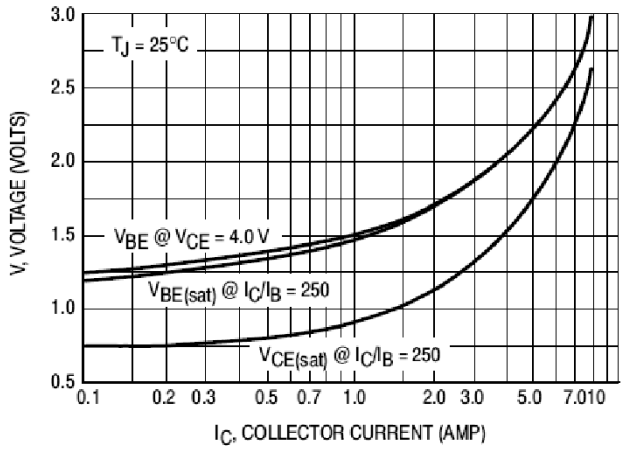
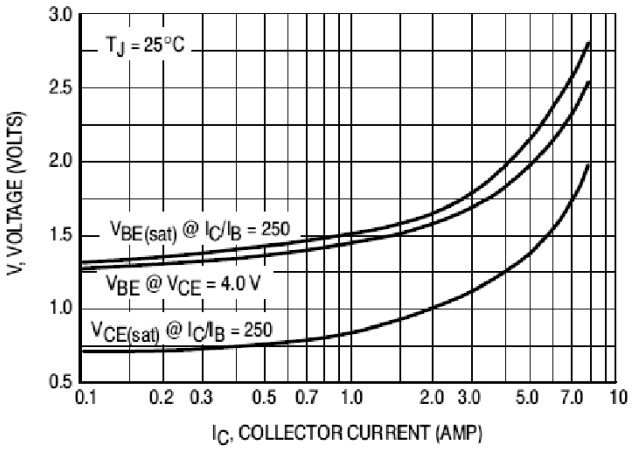


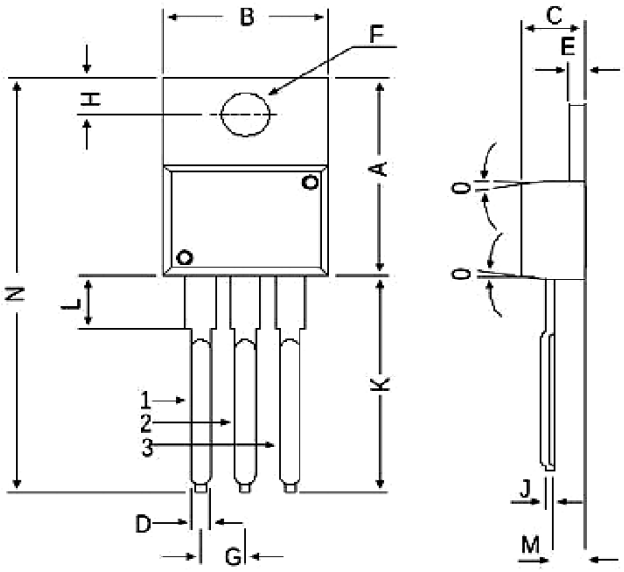
Fig 10: “On” Voltages





PACKAGE DETAILS

TO-220 Leaded Plastic Package

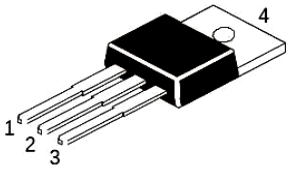


DIM	MIN	MAX
A	14.42	16.51
B	9.63	10.67
C	3.56	4.83
D	--	0.90
E	1.15	1.40
F	3.75	3.80
G	2.29	2.79
H	2.54	3.43
J	--	0.56
K	12.70	14.73
L	2.80	4.07
M	2.03	2.92
N	--	31.24
O	7°	

All Dimensions are in mm

PIN CONFIGURATION

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

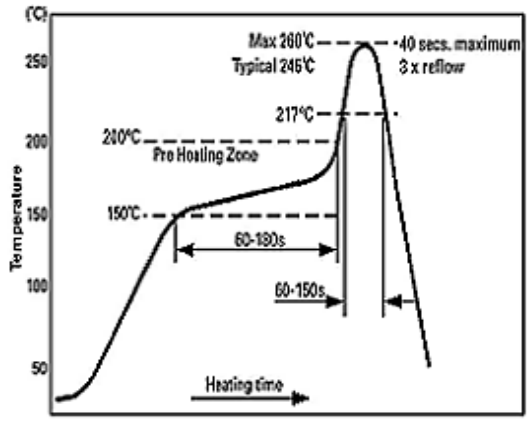
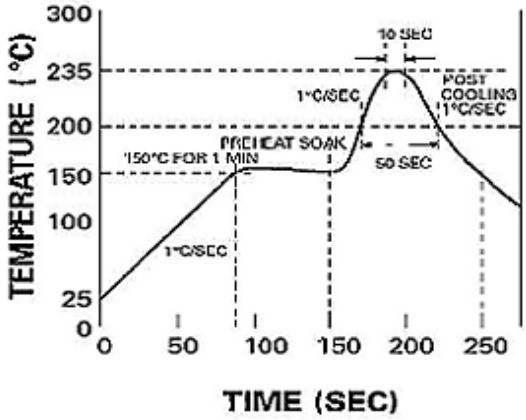


Figure 2

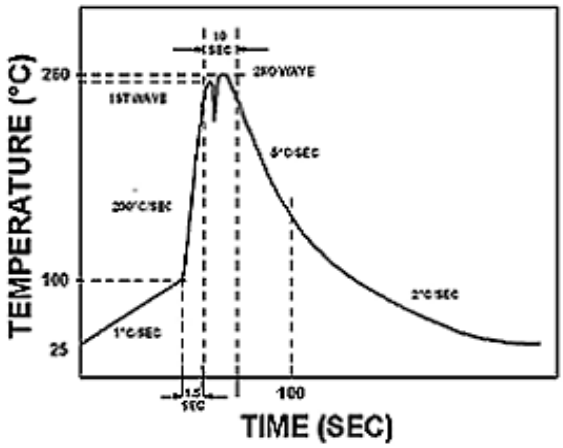


Reflow profiles in tabular form

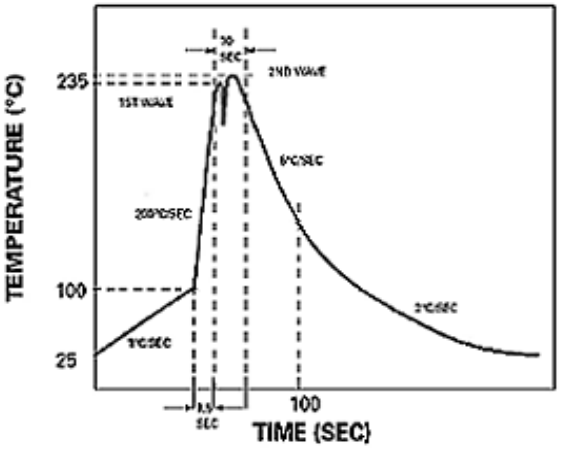
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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