PNP SILICON EPITAXIAL PLANAR TRANSISTORS BC556 ~ BC560

TO-92

TO-92 Leaded
Plastic Package
RoHS compliant

FEATURE:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

APPLICATION: For switching and AF amplifier application

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	VALUE					UNIT
		BC556	BC557	BC560	BC558	BC559	
Collector Base Voltage	V_{CBO}	80	50		30		V
Collector Emitter Voltage	V_{CEO}	65	45		30		V
Emitter Base Voltage	V_{EBO}	5					V
Collector Current (DC)	I_C	100					mA
Collector Current - Peak	I_{CM}	200					mA
Power Dissipation	P_{tot}	500					mW
Storage Temperature	T_{stg}	-65 to +150					°C
Junction Temperature	T_j	150					°C

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
DC Current Gain	h_{FE}	I_C=2mA, V_{CE}=5V	75	800	
		A	110	220	
		B	200	450	
		C	420	800	
Collector Emitter Saturation Voltage	$V_{CE(Sat)}$	I_C=10mA, I_B=0.5mA	--	0.30	V
		I_C=100mA, I_B=5mA	--	0.65	V
Base Emitter on Voltage	$V_{BE(on)}$	I_C=2mA, V_{CE}=5V	--	0.75	V
		I_C=10mA, V_{CE}=5V	--	0.82	V
Collector Base Cut off Current	I_{CBO}	V_{CB}=30V, I_E=0	--	15	nA
Emitter Base Cut off Current	I_{EBO}	V_{EB}=5V	--	100	nA
Collector Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100µA			V
BC556			80	--	
BC557 , BC560			50	--	
BC558 , BC559			30	--	
Collector Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=2mA		--	V
BC556			65	--	
BC557 , BC560			45	--	
BC558 , BC559			30	--	
Emitter Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=100µA	5	--	V
Transition Frequency	f_T		100	--	HMz
Collector Base Capacitance	C_{cb}	V_{CB}=10V, f=1MHz	--	6.0	pF

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

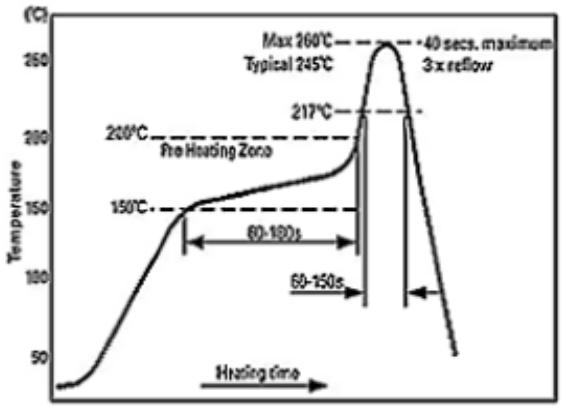
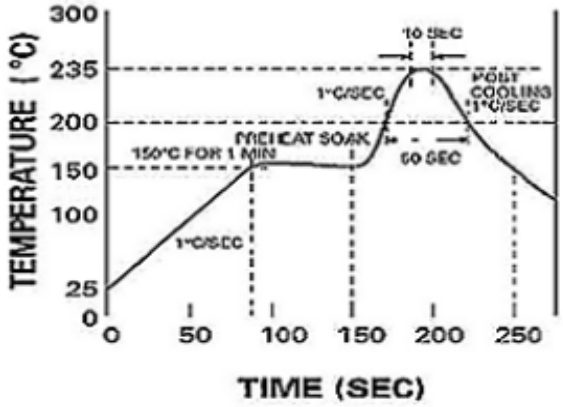


Figure 2

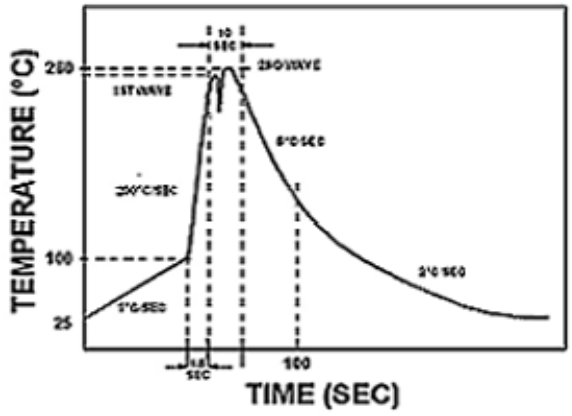


Reflow profiles in tabular form

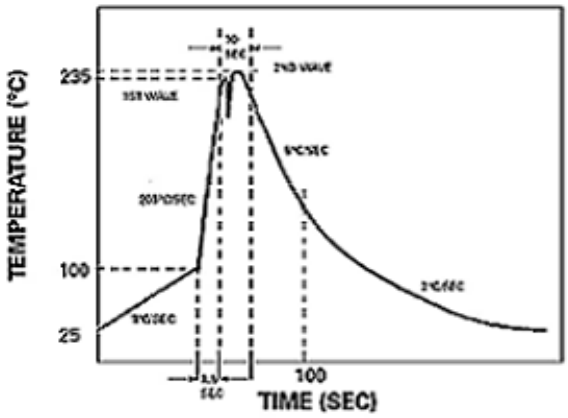
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: Normalized DC Current Gain

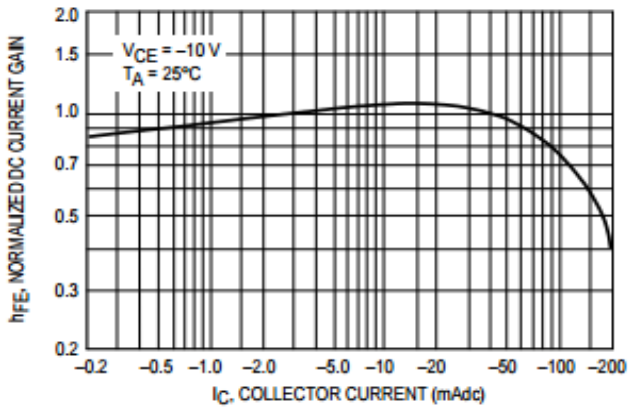


Fig 2: Collector Saturation Region

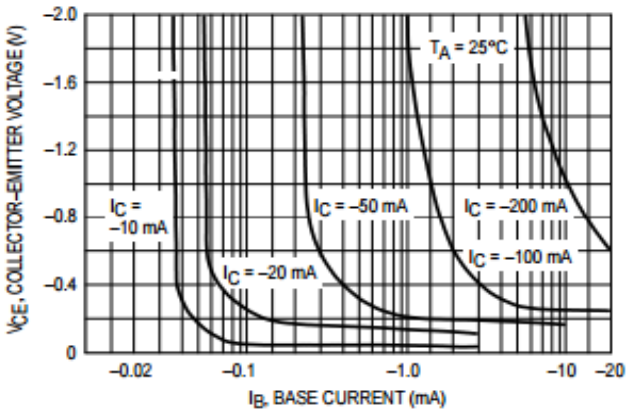


Fig 3: Capacitance

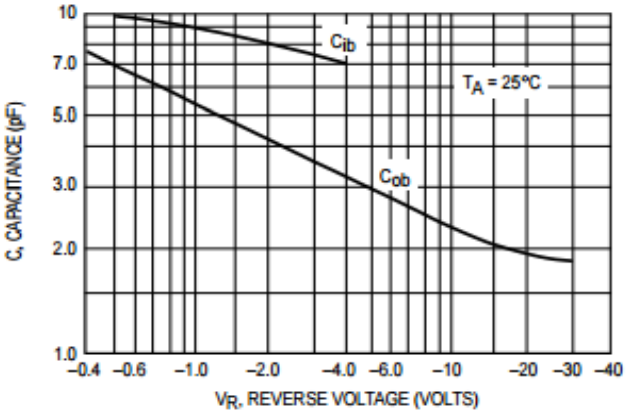


Fig 4: “Saturation” and “On” Voltages

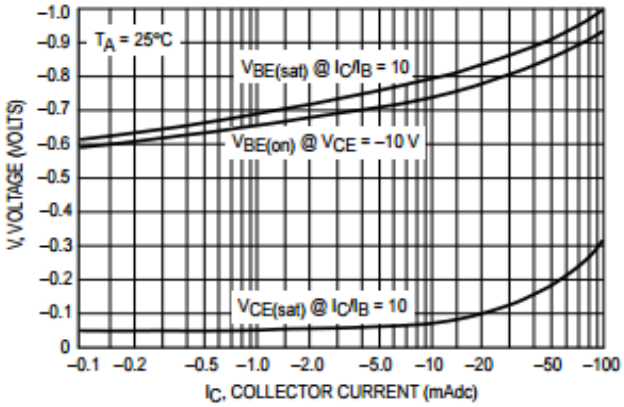


Fig 5: Base–Emitter Temperature Coefficient

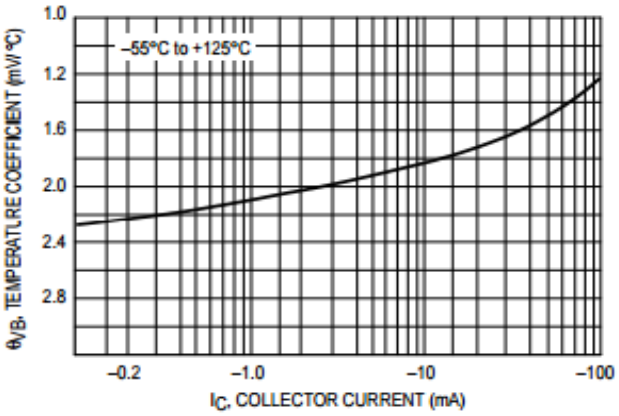
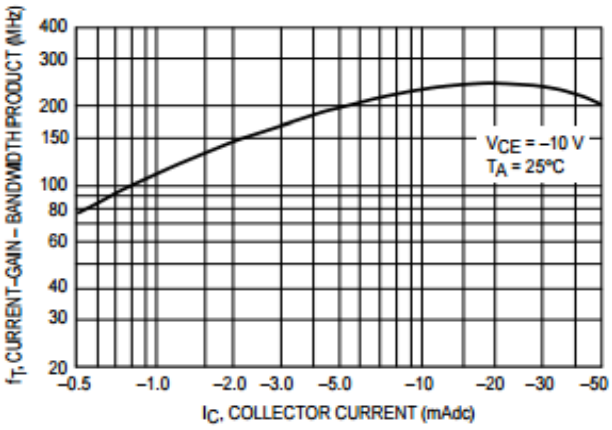


Fig 6: Current–Gain – Bandwidth Product



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TYPICAL CHARACTERISTICS CURVES

Fig 7: DC Current Gain

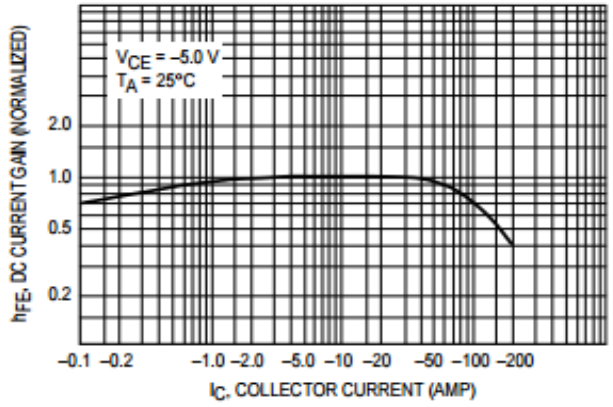


Fig 8: Collector Saturation Region

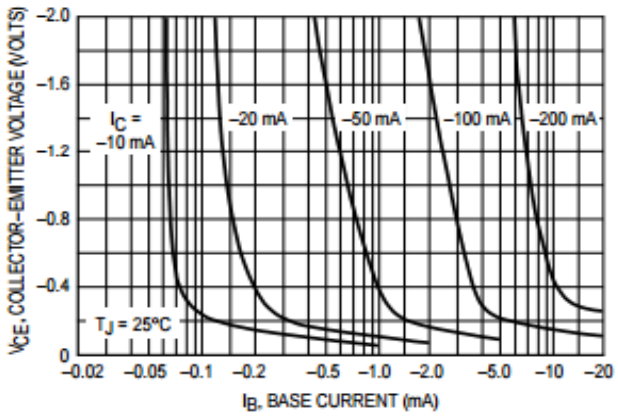


Fig 9: Capacitance

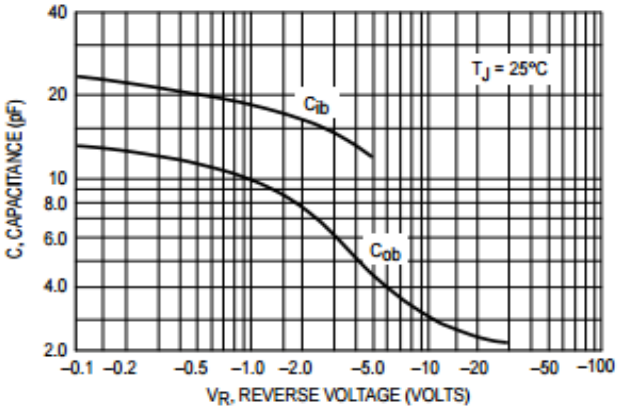


Fig 10: “On” Voltage

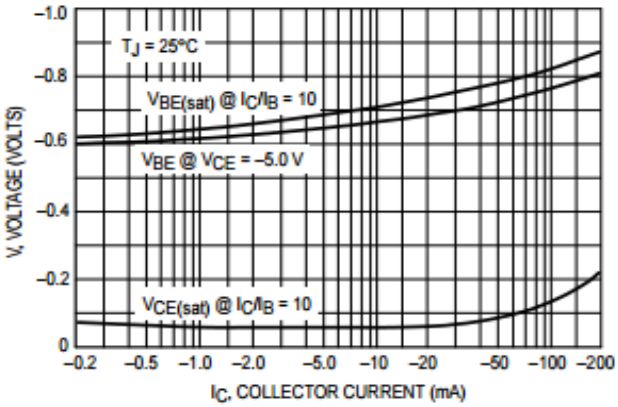


Fig 11: Base–Emitter Temperature Coefficient

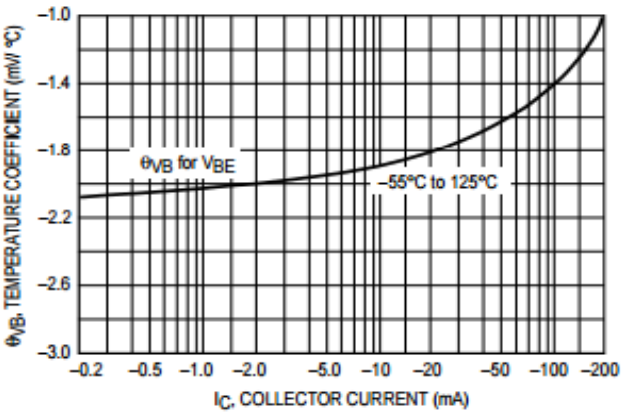
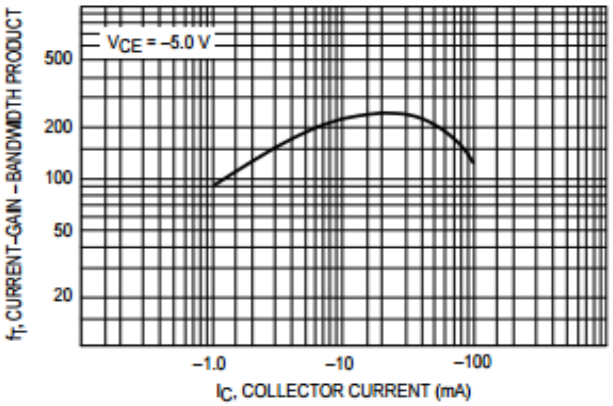


Fig 12: Current–Gain – Bandwidth Product



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TYPICAL CHARACTERISTICS CURVES

Fig 13: Thermal Response

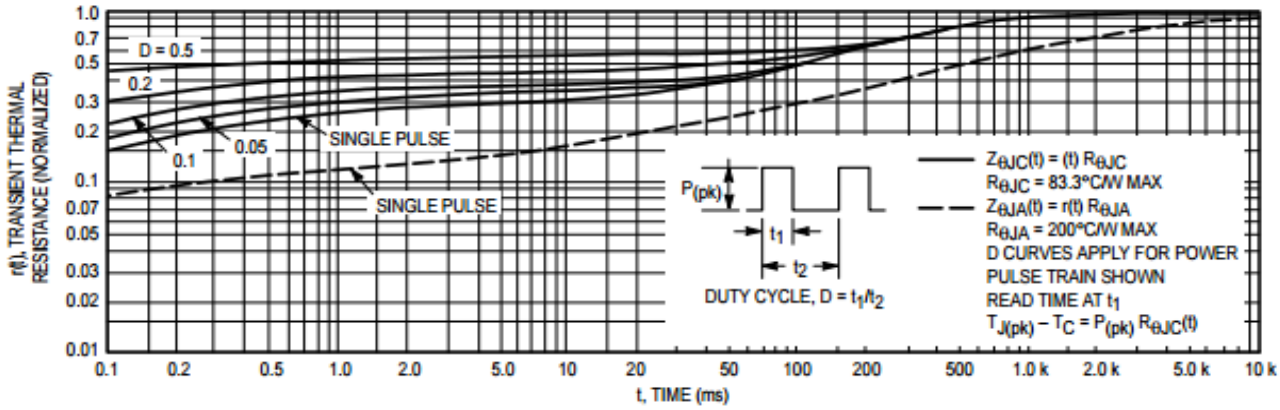
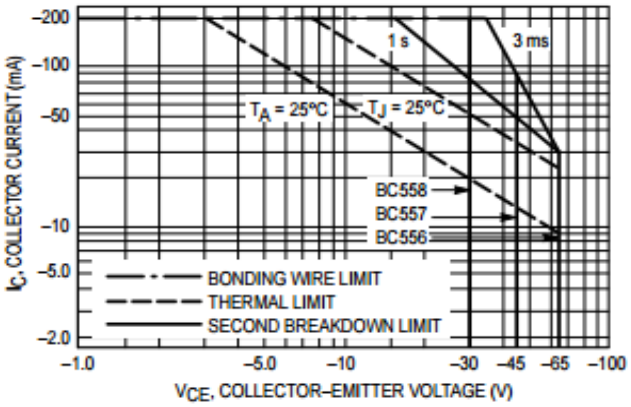
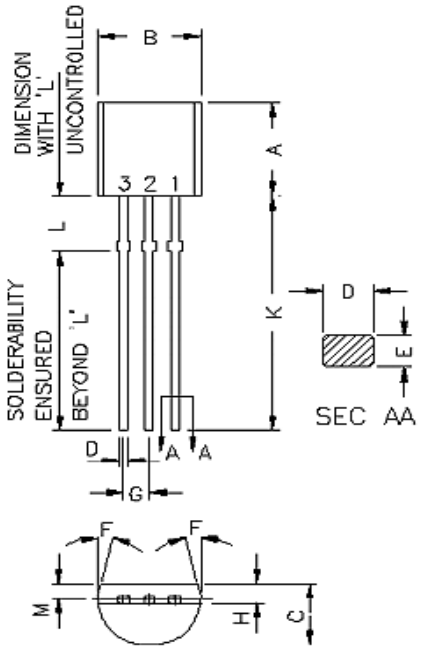


Fig 14: Active Region — Safe Operating Area



PACKAGE DETAILS

TO-92 Plastic Package



DIM	MIN	MAX
A	4.30	5.33
B	4.10	5.20
C	3.10	4.19
D	0.35	0.55
E	0.29	0.55
F	8 DEG	
G	1.14	1.40
H	1.00	1.80
K	11.50	--
L	1.982	2.082
M	1.03	1.53

All dimensions are in mm

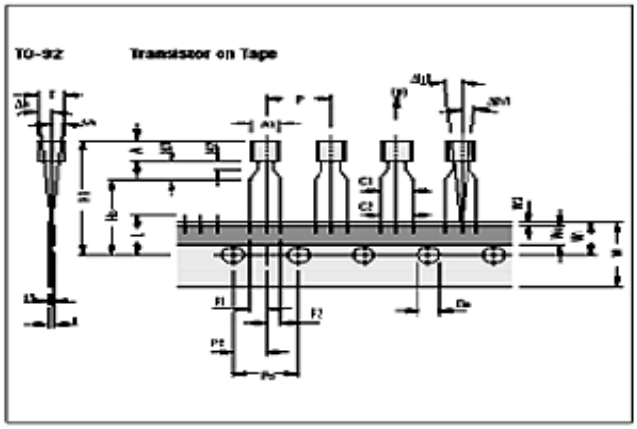
Package Specifications:

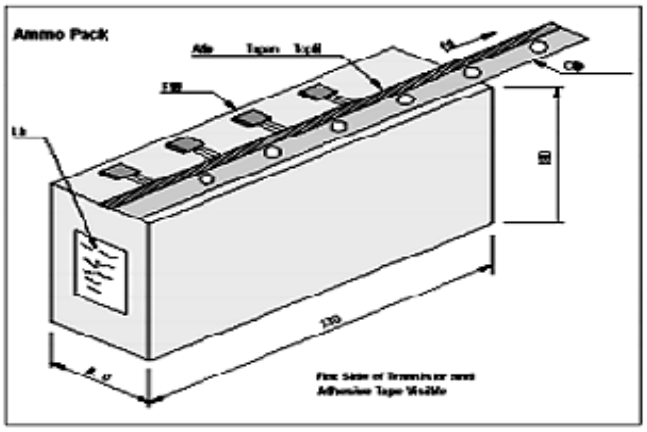
T & A: Tape and Ammo Pack; T & R: Tape and Reel; **Bulk**: Loose in Poly Bags; **Tube**: Tube and Carton; Kit 1,000

Package / Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19 x 19 x 8	1.1	80K	43 x 40 x 35	20.0
	T & A	2,000	2K	32 x 4.5 x 20	0.7	40K	43 x 40 x 35	15.2

PACKAGE DETAILS

TO-92 and TO-92L Tape and Ammo Package





All dimensions are in mm

Tape Specifications

ITEM	SYMBOL	SPECIFICATION			
		MIN.	NOM.	MAX.	TOL.
BODY WIDTH	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component[cr]	P		12.7		±1.0
Feed hole pitch[§1]	Po		12.7		±0.3
Feed hole centre to component centre[§2]	P2		6.35		±0.4
Comp. alignment,side view[§3]	Dh		0	1.0	
Comp. alignment,front view[§3]	Dh1		0	1.3	
Tape width[cr]	W		18		±0.5
Hole-down tape width[cr]	Wo		6		±0.2
Hole position	W1		9		±0.7-0.5
Hole-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of snipped leads	L			11.0	
Feed hole diameter[cr]	Do		4		±0.2
Total tape thickness[§4]	t			1.2	
Lead-to-lead distance[cr]	F1,F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelism[cr]	C1-C2			0.22	
pull-out force	(p)	6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feedholes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of achesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.
§2 To be measured at bottom of clinch.
§3 At top of body.
§4 t1 = 0.3 – 3.6 mm
Cr Critical Dimension.

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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