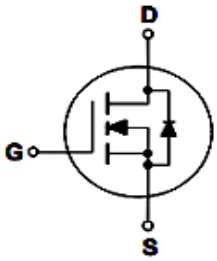
N-Channel Plastic-Encapsulate MOSFET

BS170

60V , 500mA

TO-92



TO-92
Plastic Package
RoHS compliant

FEATURES:

1. High Density Cell Design for Low $R_{DS(ON)}$
2. Voltage Controlled Small Signal Switch
3. Rugged and reliable
4. High saturation current capability

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source voltage		V_{DSS}	60	V
Drain-Gate Voltage (R_{GS}≤1MΩ)		V_{DGR}	60	V
Gate-Source voltage		V_{GSS}	±20	V
Drain Current	Continuous	I_D	500	mA
	Pulsed		1200	
Maximum Power Dissipation		P_D	830	mW
Derate Above 25°C			6.6	mW/°C
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds		T_L	300	°C

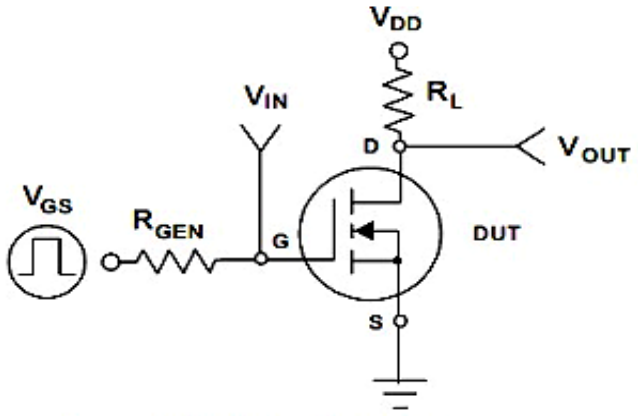
THERMAL RESISTANCE

Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	150	°C/W

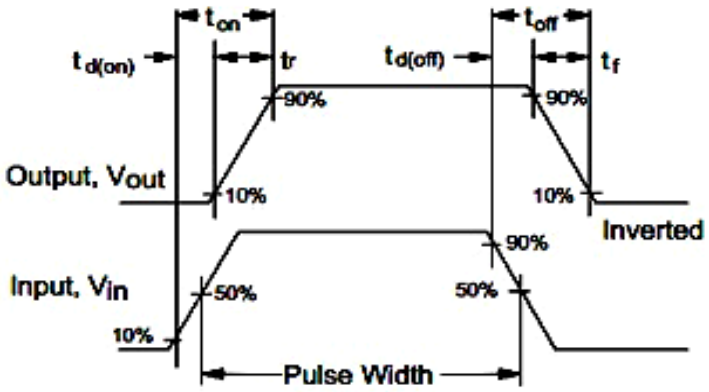
ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0V, I_D = 100μA	60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25V, V_{GS} = 0V	--	--	0.5	μA
Gate-body Leakage	I_{GSF}	V_{GS} = 15V, V_{DS}= 0V,	--	--	10	nA
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1mA	0.8	2.1	3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} =10V, I_D = 200mA	--	1.2	5	Ω
Forward Trans conductance	g_{fs}	V_{DS} =10V, I_D =200mA	--	320	--	mS
Input Capacitance	C_{iss}	V_{GS} = 0V	--	24	40	pF
Output Capacitance	C_{oss}	V_{DS} = 10V	--	17	30	
Reverse Transfer Capacitance	C_{rss}	f = 1.0MHz	--	7	10	
Turn-On Time	$t_{d(on)}$	V_{DD}= 25V, I_D= 200mA,	--	--	10	ns
Turn-Off Time	$t_{d(off)}$	V_{GS}= 10V, R_{GEN} = 25W	--	--	10	

TEST CIRCUIT AND DIAGRAMS



Switching Test Circuit



Switching Waveforms

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

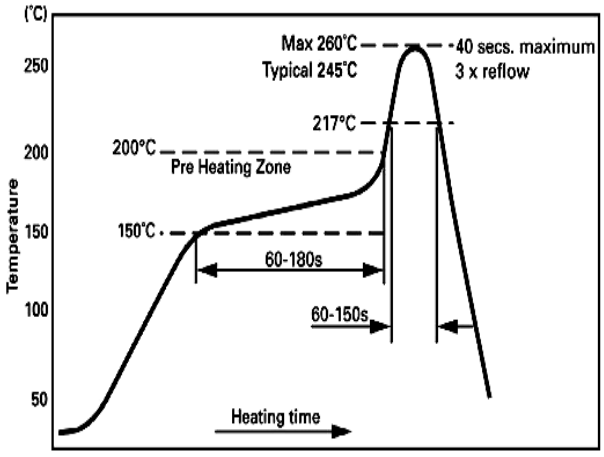
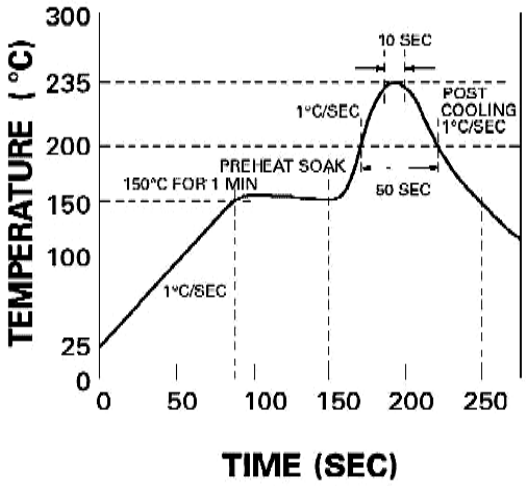


Figure 2

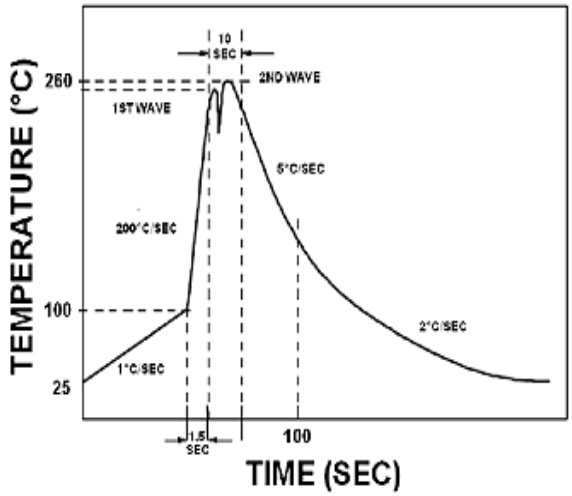


Reflow profiles in tabular form

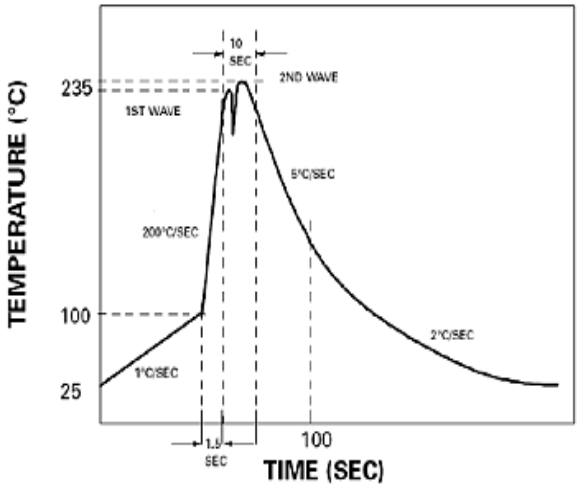
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form		
Profile Feature	**Sn-Pb System**	**Pb-Free System**
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: On-Region Characteristics

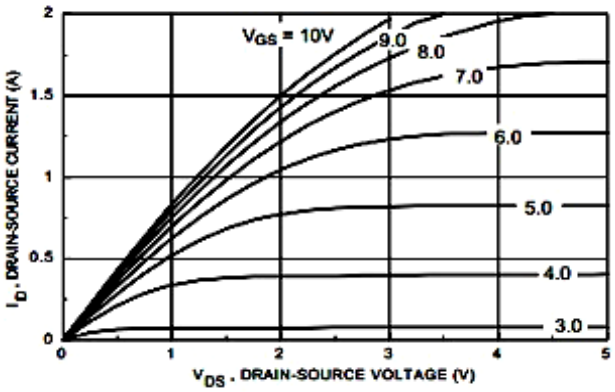


Fig 2: On-Resistance Variation with Temperature

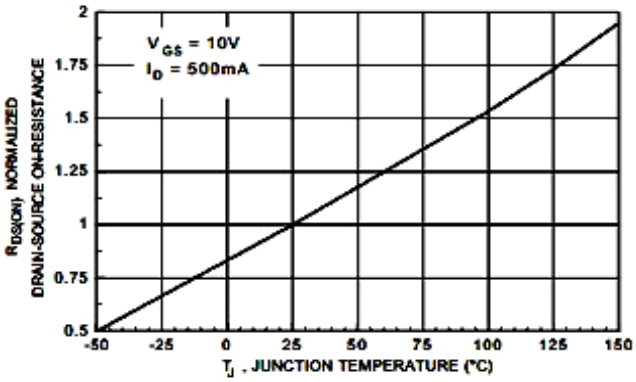


Fig 3: Transfer Characteristics

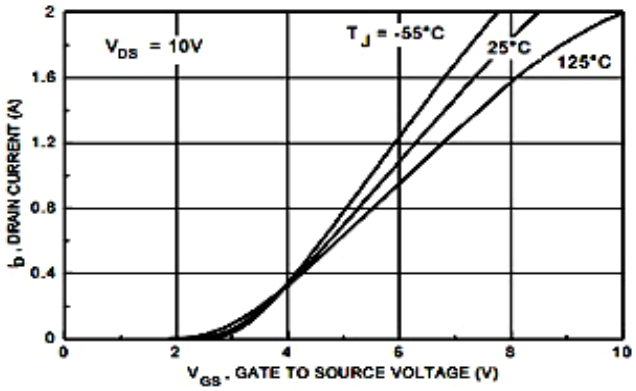


Fig 4: On-Resistance Variation with Gate Voltage and Drain Current

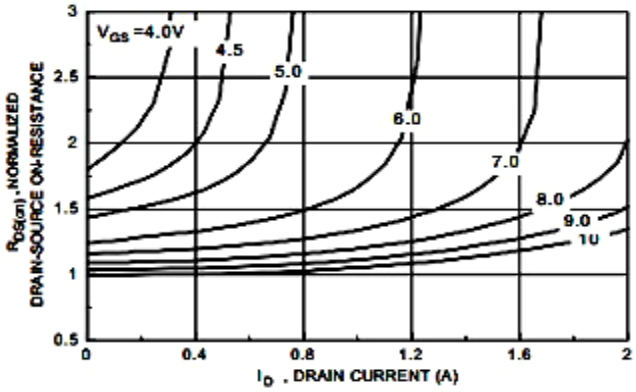


Fig 5: On-Resistance Variation with Drain Current and Temperature

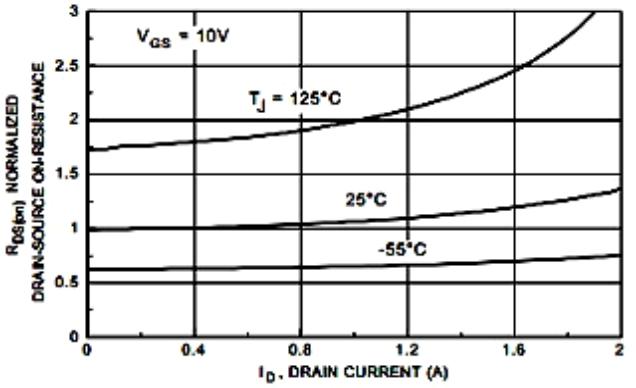
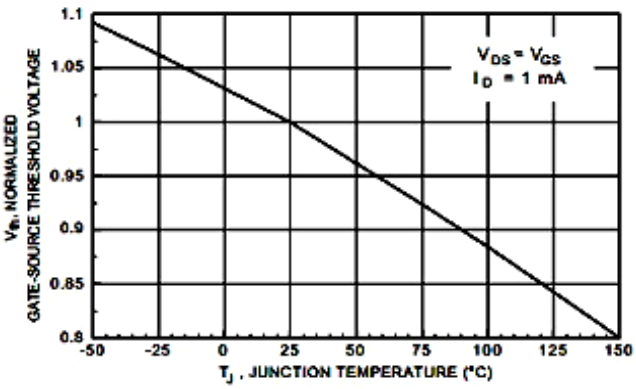


Fig 6: Gate Threshold Variation with Temperature



TYPICAL CHARACTERISTICS CURVES

Fig 7: Breakdown Voltage Variation with Temperature

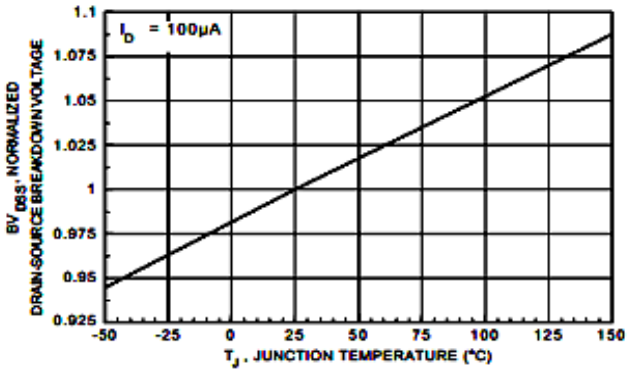


Fig 8: Capacitance Characteristics

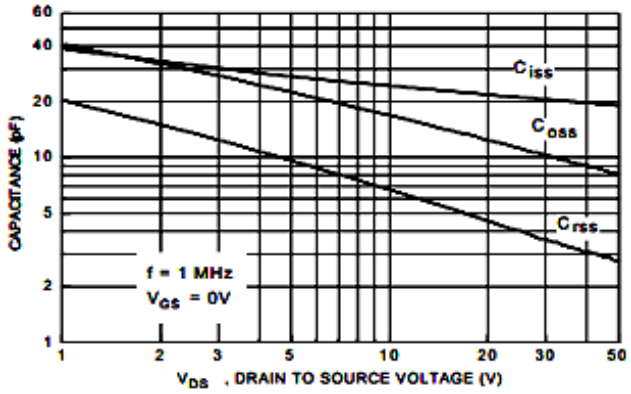


Fig 9: BS170 Maximum Safe Operating Area

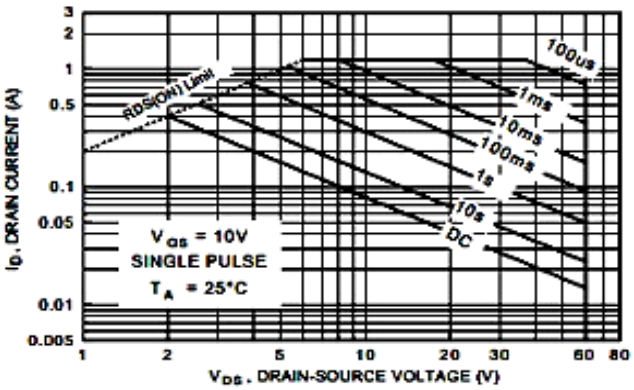


Fig 10: Body Diode Forward Voltage Variation with Current and Temperature

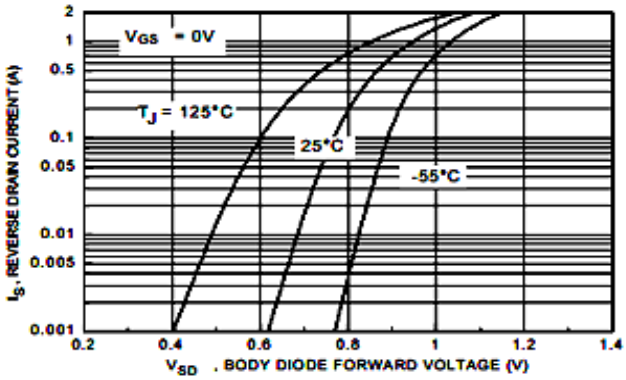


Fig 11: Gate Charge Characteristics

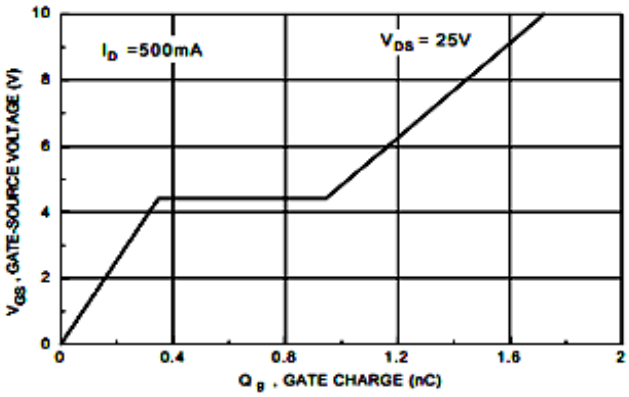
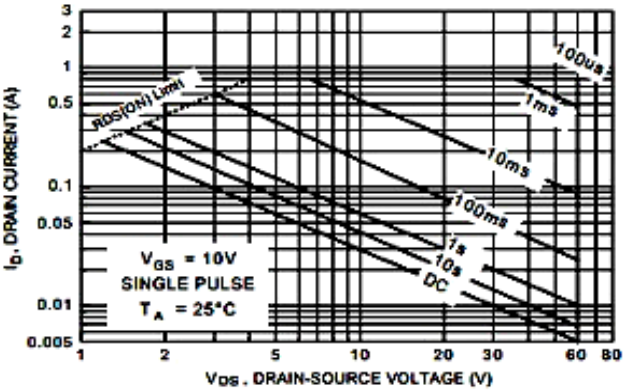
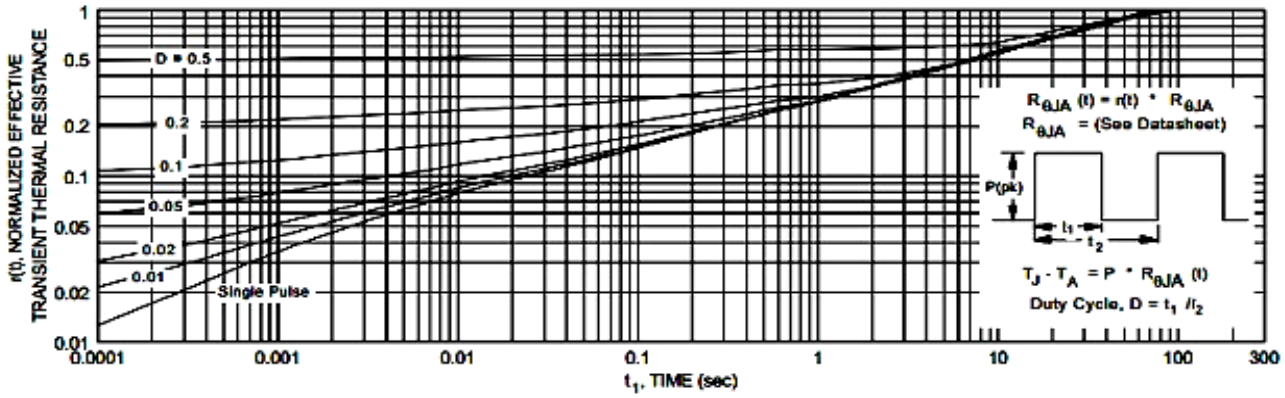


Fig 12: MMBF 170 Maximum Safe Operating Area



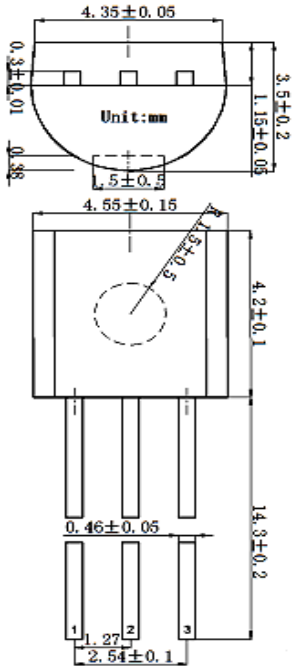
TYPICAL CHARACTERISTICS CURVES

Fig 13: TO-92, BS170 Transient Thermal Response Curve



PACKAGE DETAILS

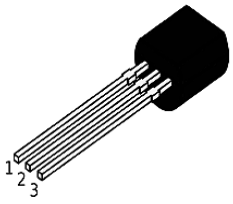
TO-92 Plastic Package



All dimensions are in mm

Pin Configuration

1. Drain
2. Gate
3. Source



Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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Continental Device India Pvt. Limited
C-120 Naraina Industrial Area, New Delhi 110 028, India.
Telephone +91-11-2579 6150, 4141 1112 Fax +91-11-2579 5290, 4141 1119
email@cdil.com www.cdil.com
CIN No. U32109DL1964PTC004291

BS170
Rev0 24112021EJS