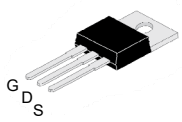
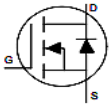
N-Channel POWER MOSFET

CD4132



TO-220



TO-220 Leaded
Plastic Package
RoHS compliant

FEATURES:

1. Best in Class Performance for UPS/Inverter Applications
2. Very Low $R_{DS(on)}$ at 4.5V V_{GS}
3. Ultra-Low Gate Impedance
4. Fully Characterized Avalanche Voltage and Current
5. Lead-Free, RoHS Compliant

V_{DSS}	30	V
$R_{DS(on)}$ max (@ V_{GS} = 10V)	3.5	mΩ
(@ V_{GS} = 4.5V)	4.5	
Q_g (typical)	36	nC
$I_{D\ (Silicon\ Limited)}$	150 [4]	A
$I_{D\ (Package\ Limited)}$	78	

APPLICATION:

1. Optimized for UPS/Inverter Applications
2. Low Voltage Power Tools

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETERS	SYMBOL	VALUE	UNIT
Drain-to-Source Voltage	V_{DS}	30	V
Gate-to-Source Voltage	V_{GS}	±20	V
Continuous Drain Current, V_{GS} @ 10V (Silicon Limited) @ T_C = 25°C	I_D	150 [4]	A
Continuous Drain Current, V_{GS} @ 10V (Silicon Limited) @ T_C = 100°C	I_D	100	
Continuous Drain Current, V_{GS} @ 10V (Package Limited) @ T_C = 25°C	I_D	78	
Pulsed Drain Current [1]	I_{DM}	620	
Maximum Power Dissipation [6] @T_C = 25°C	P_D	140	W
Maximum Power Dissipation [6] @T_C = 100°C	P_D	68	W
Linear Derating Factor		0.90	W/°C
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 to +175	°C
Soldering Temperature, for 10 seconds (1.6mm from case)	--	300	
Mounting Torque, 6-32 or M3 Screw	--	10 lbf·in (1.1 N·m)	

THERMAL RESISTANCE

PARAMETER	SYMBOL	TYP	MAX	UNIT
Junction-to-Case [6]	$R_{\theta JC}$	--	1.11	°C/W
Case-to-Sink, Flat Greased Surface	$R_{\theta CS}$	0.50	--	
Junction-to-Ambient [5]	$R_{\theta JA}$	--	62	

ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	30	--	--	V
Breakdown Voltage Temp. Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C, I_D = 1mA [1]	--	17	--	mV/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 40A [3]	--	2.5	3.5	mΩ
		V_{GS} = 4.5V, I_D = 32A [3]	--	3.5	4.5	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 100µA	1.35	1.8	2.35	V
Gate Threshold Voltage Coefficient	$\Delta V_{GS(th)}/\Delta T_J$		--	-7.7	--	mV/°C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} =24V, V_{GS} = 0V	--	--	1.0	µA
		V_{DS} =24V,V_{GS} = 0V,T_J =125°C	--	--	100	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	--	--	100	nA
Gate-to-Source Reverse Leakage		V_{GS} = -20V	--	--	-100	
Forward Transconductance	g_{fs}	V_{DS} = 15V, I_D =32A	190	--		S
Total Gate Charge	Q_g	V_{DS} = 15V V_{GS} = 4.5V I_D = 32A	--	36	54	nC
Pre-Vth Gate-to-Source Charge	Q_{gs1}		--	9.1	--	
Post-Vth Gate-to-Source Charge	Q_{gs2}		--	4.2	--	
Gate-to-Drain Charge	Q_{gd}		--	13	--	
Gate Charge Overdrive	Q_{godr}		--	13	--	
Switch Charge (Qgs2 + Qgd)	Q_{sw}		--	17.2	--	
Output Charge	Q_{oss}	V_{DS} = 16V, V_{GS} = 0V	--	21	--	nC
Gate Resistance	R_G		--	0.85	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V I_D = 32A R_G= 1.8Ω V_{GS} = 4.5V [3]	--	23	--	ns
Rise Time	t_r		--	92	--	
Turn-Off Delay Time	$t_{d(off)}$		--	25	--	
Fall Time	t_f		--	36	--	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 15V f = 1.0MHz	--	5110	--	pF
Output Capacitance	C_{oss}		--	960	--	
Reverse Transfer Capacitance	C_{rss}		--	440	--	
Avalanche Characteristics						
Single Pulse Avalanche Energy [2]	E_{AS} (Thermally limited)	310				mJ
Single Pulse Avalanche Energy Tested Value [7]	E_{AS} (tested)	900				
Avalanche Current [1]	I_{AR}	32				A
Repetitive Avalanche Energy [1]	E_{AR}	14				mJ

ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise specified)

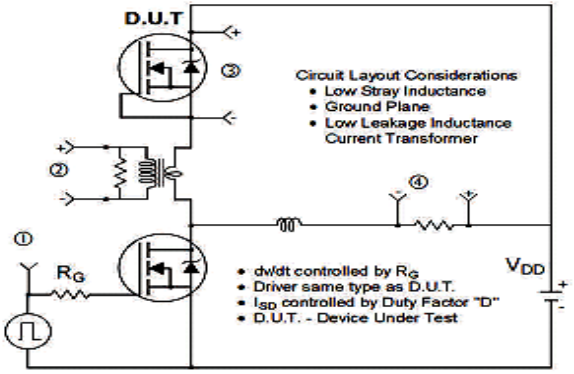
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.	--	--	150 [4]	A
Pulsed Source Current (Body Diode)	I_{SM}		--	--	620	
Diode Forward Voltage	V_{SD}	T_J = 25°C,I_S = 32A,V_{GS} = 0V [1]	--	--	1.0	V
Reverse Recovery Time	t_{rr}	T_J = 25°C I_F = 32A ,V_{DD}=15V	--	29	44	ns
Reverse Recovery Charge	Q_{rr}	di/dt = 200A/µs [3]	--	49	74	nC

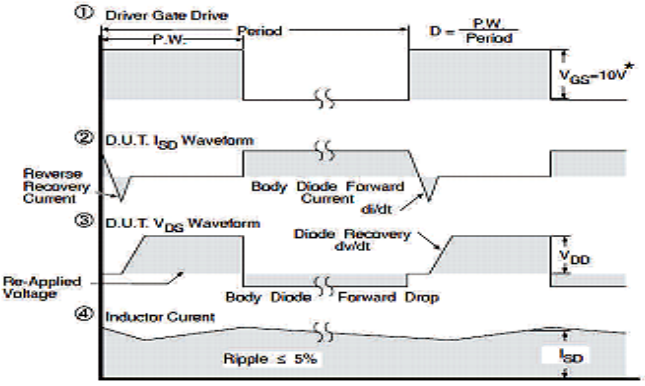
Note:

1. Repetitive rating; pulse width limited by max. junction temperature.
2. Limited by T_{Jmax}, starting T_J = 25°C, L = 0.61mH, R_G = 25Ω, I_{AS} = 32A.
3. Pulse width ≤ 400µs; duty cycle ≤ 2%
4. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 78A
5. When mounted on 1" square PCB (FR-4 or G-10 Material).
6. Rθ is measured at T_J approximately 90°C.
7. Starting T_J =25°C, L=0.50mH, RG = 25Ω, I_{AS} =60A, V_{DD} =25V. (Statistical Limit)

TEST CIRCUIT AND DIAGRAMS

Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET Power MOSFETs

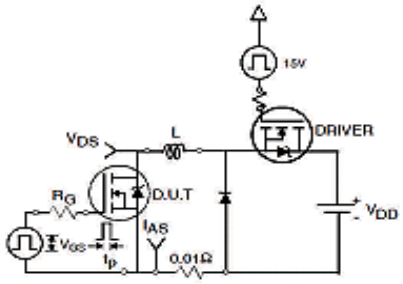


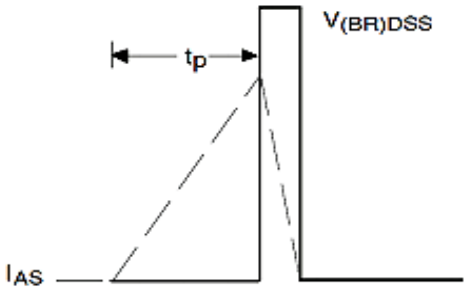


* V_{GS} = 5V for Logic Level Devices

Unclamped Inductive Test Circuit

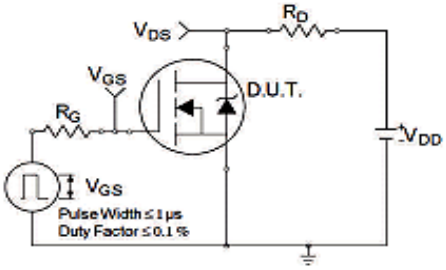
Unclamped Inductive Waveforms

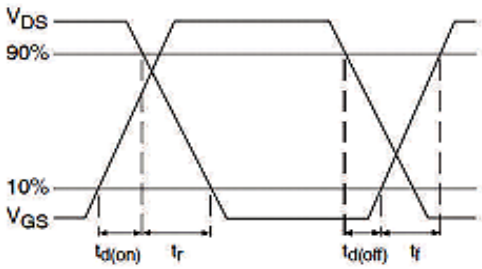




Switching Time Test Circuit

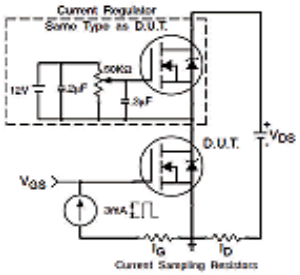
Switching Time Waveforms

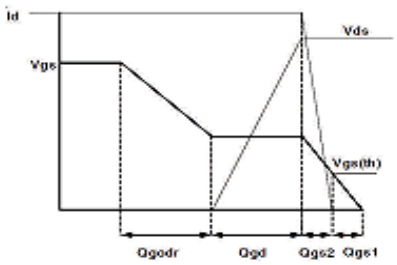




Gate Charge Test Circuit

Gate Charge Waveform





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TYPICAL CHARACTERISTICS CURVES

Fig 1: Typical Output Characteristics

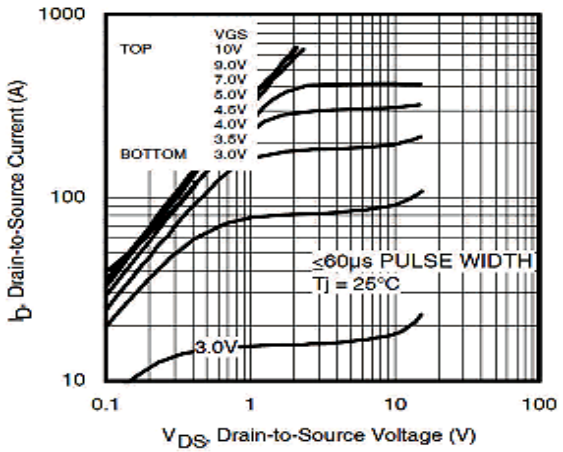


Fig 2: Typical Transfer Characteristics

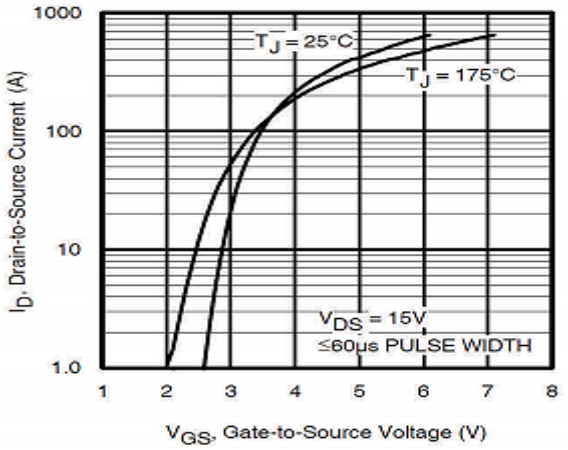


Fig 3: Typical Capacitance vs. Drain-to-Source Voltage

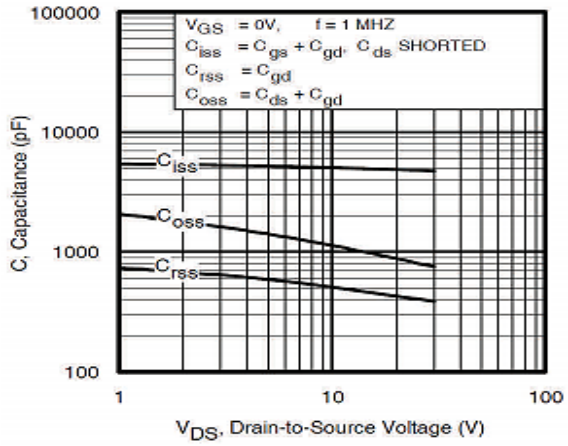


Fig 4: Typical Output Characteristics

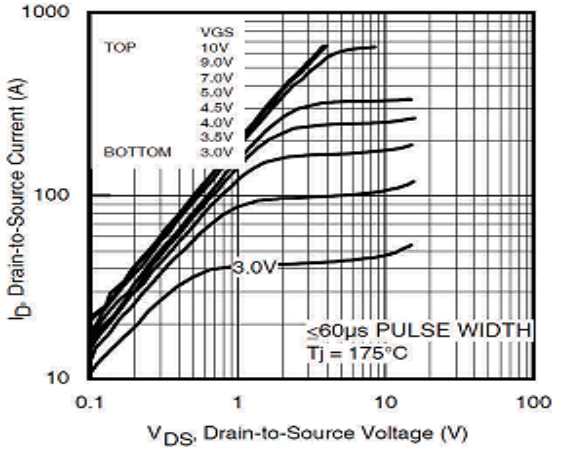


Fig 5: Normalized On-Resistance vs. Temperature

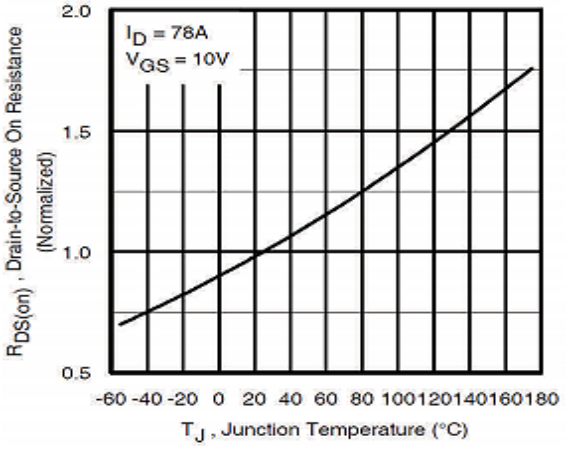
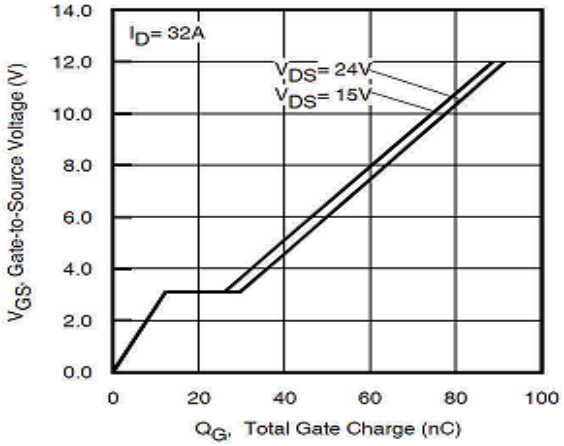


Fig 6: Typical Gate Charge vs. Gate-to-Source Voltage



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TYPICAL CHARACTERISTICS CURVES

Fig 7: Typical Source-Drain Diode Forward Voltage

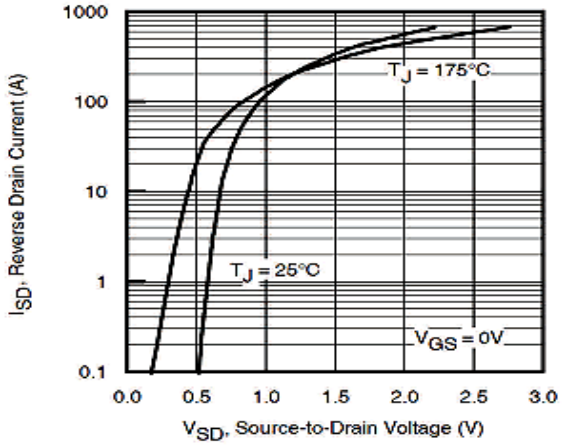


Fig 8: Maximum Drain Current vs. Case Temp

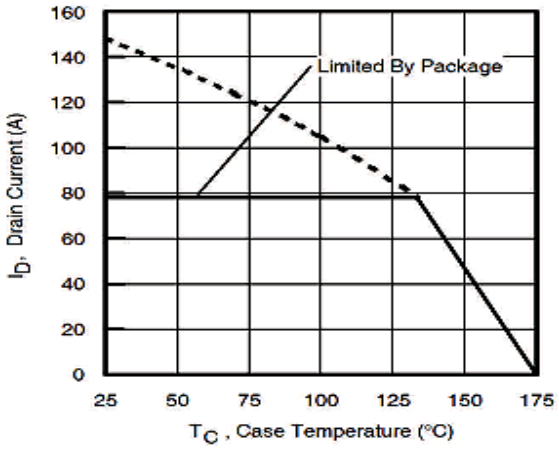


Fig 9: Typical On-Resistance vs. Gate Voltage

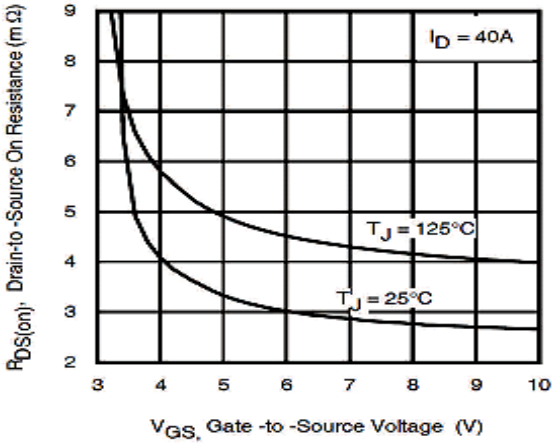


Fig 10: Maximum Safe Operating Area

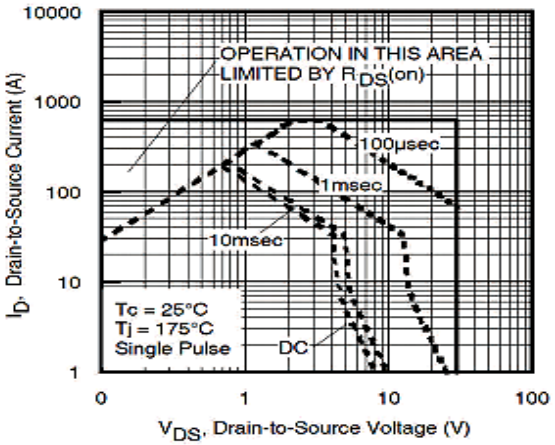


Fig 11: Threshold Voltage vs. Temp

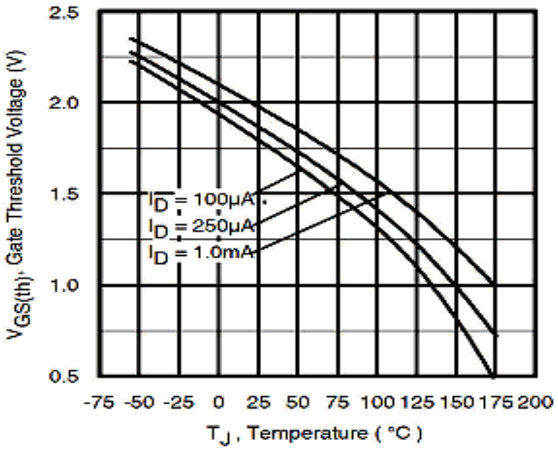
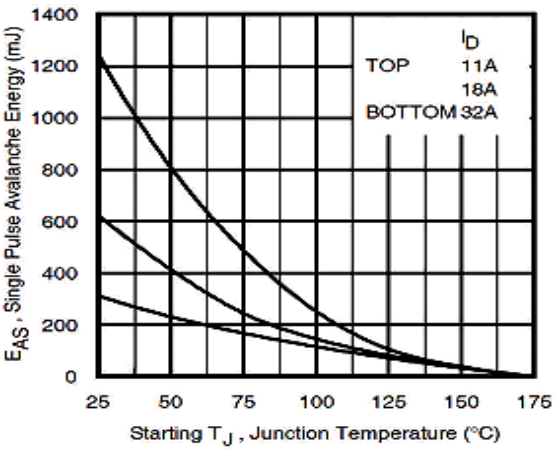


Fig 12: Maximum Avalanche Energy vs. Drain Current



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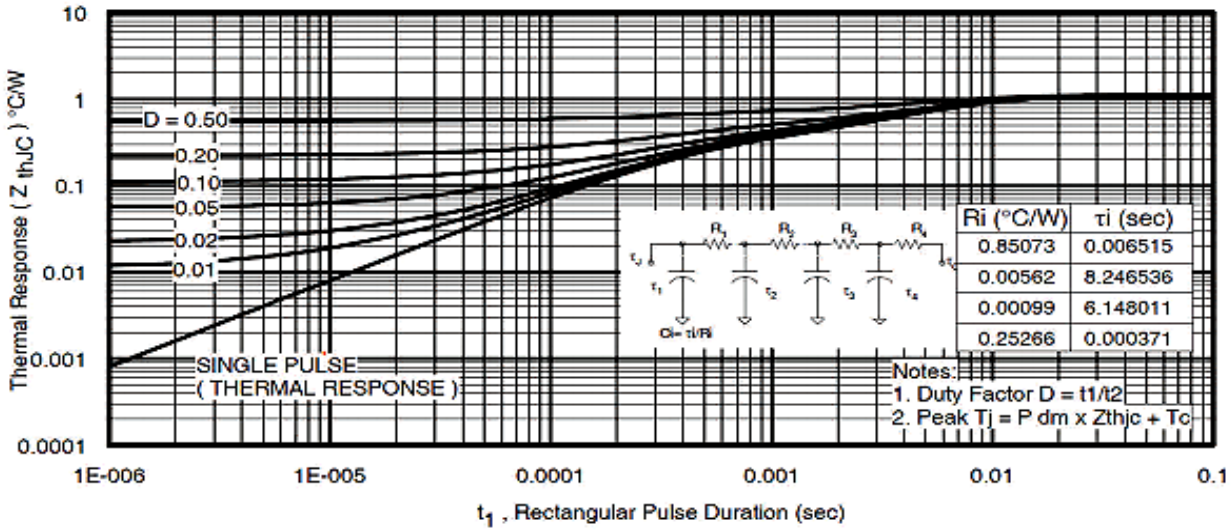
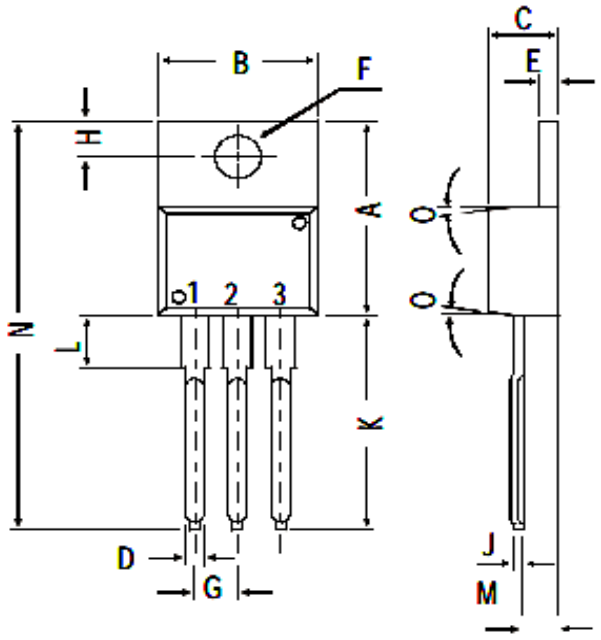
TYPICAL CHARACTERISTICS CURVES

Fig 13: Maximum Effective Transient Thermal Impedance, Junction-to-Case



PACKAGE DETAILS

TO-220 Package Outline and Dimension

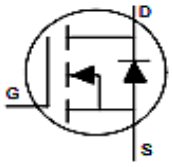


DIM	MIN	MAX
A	14.42	16.51
B	9.63	10.67
C	3.56	4.83
D		0.90
E	1.15	1.40
F	3.75	3.88
G	2.29	2.79
H	2.54	3.43
J		0.56
K	12.70	14.73
L	2.80	4.07
M	2.03	2.92
N		31.24
O	7°	

All Dimensions are in mm

Pin Configurations

1. Gate
2. Drain
3. Source



Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

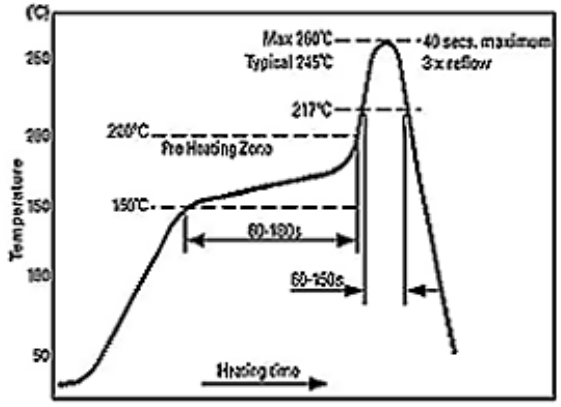
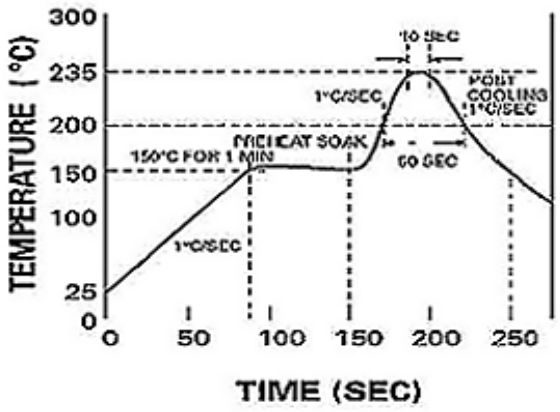


Figure 2

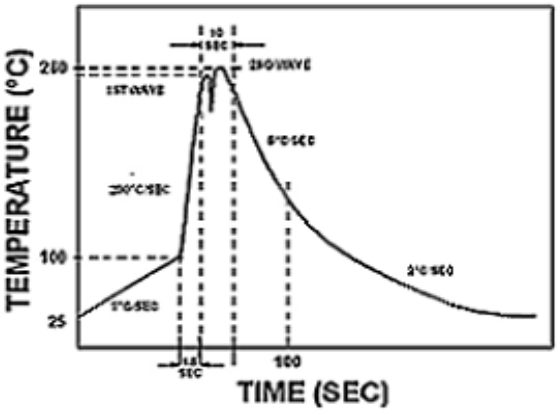


Reflow profiles in tabular form

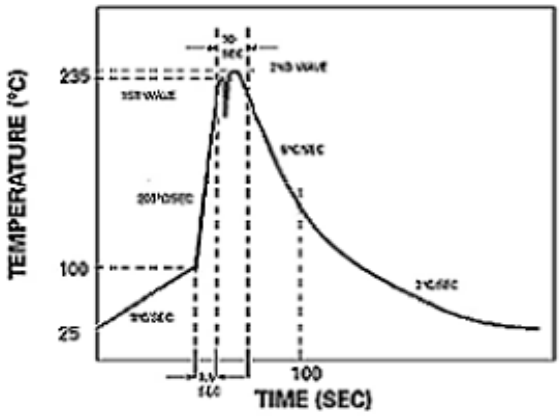
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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