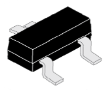
P-Channel Power MOSFET

CDM6401



SOT-23

SOT-23
SMD Package
RoHS compliant

FEATURES:

1. Ultra Low On-Resistance
2. Low Profile (<1.1mm)
3. Available in Tape and Reel
4. Fast Switching
5. 1.8V Gate Rated
6. Lead-Free
7. Halogen-Free
8. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products , please suffix - AQ in the part number while ordering

ABSOLUTE MAXIMUM RATING (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage		V_{DS}	12	V
Continuous Drain Current, V_{GS} @ 4.5V	@ T_A = 25°C	I_D	4.3	A
Continuous Drain Current, V_{GS} @ 4.5V	@ T_A = 70°C	I_D	3.4	A
Pulsed Drain Current [1]		I_{DM}	34	A
Maximum Power Dissipation	@T_A = 25°C	P_D	1.3	W
Maximum Power Dissipation	@T_A = 70°C	P_D	0.8	W
Linear Derating Factor			0.01	W/°C
Single Pulse Avalanche Energy [4]		E_{AS}	33	mJ
Gate-to-Source Voltage		V_{GS}	±8	V
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

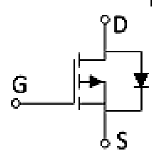
Thermal Resistance

PARAMETER	SYMBOL	TYP	MAX	UNIT
Maximum Junction-to-Ambient [3]	$R_{\theta JA}$	75	100	°C/W

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Drain-to-Source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	12	--	--	V
Breakdown voltage temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D=-1mA	--	0.007	--	V/°C
Static drain-to-source on-resistance	$R_{DS(on)}$	V_{GS} =-4.5V, I_D = -4.3A [2]	--	--	50	mΩ
		V_{GS} =-2.5V, I_D = -2.5A [2]	--	--	85	mΩ
		V_{GS} =-1.8V, I_D = -2.0A [2]	--	--	125	mΩ
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	0.40	0.55	0.95	V
Forward Trans conductance	g_{fs}	V_{DS} =-10V, I_D = -4.3A	8.6	--	--	S
Drain-to-Source leakage current	I_{DSS}	V_{DS} =-12V, V_{GS} = 0V	--	--	1.00	μA
		V_{DS}=-9.6V,V_{GS}=0V,T_J=55°C	--	--	25	μA
Gate-to-Source forward leakage	I_{GSS}	V_{GS} = -8V	--	--	100	nA
Gate-to-Source reverse leakage		V_{GS} = -8V	--	--	100	nA
Total Gate Charge	Q_g	I_D = -4.3A,V_{DS} = -10V V_{GS} = -5.0V [2]	--	10	15	nC
Gate-to-Source Charge	Q_{gs}		--	1.4	2.1	
Gate-to-Drain ("Miller") Charge	Q_{gd}		--	2.6	3.9	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} =-6.0V,I_D = -1.0A R_G = 89Ω, RD = 6.0Ω 2)	--	11	--	ns
Rise Time	t_r		--	32	--	
Turn-Off Delay Time	$t_{d(off)}$		--	250	--	
Fall Time	t_f		--	210	--	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = -10V f = 1.0MHz	--	810	--	pF
Output Capacitance	C_{oss}		--	180	--	
Reverse Transfer Capacitance	C_{rss}		--	125	--	

Source-Drain Ratings and Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse P-N junction diode 	--	--	1.3	A
Pulsed Source Current (Body Diode) [1]	I_{SM}		--	--	34	A
Diode Forward Voltage	V_{SD}	T_J=25°C, I_S=-1.3A, V_{GS}=0V [2]	--	--	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F=-1.3A, di/dt = -100A/μs 2)	--	22	33	ns
Reverse Recovery Charge	Q_{rr}		--	8	12	nC

Note:

1. 1.Repetitive rating; pulse width limited by max. Junction temperature.
2. Pulse width ≤ 300μs; duty cycle ≤ 2%
3. Surface mounted on 1" square single layer 1 oz. copper FR4 board, steady state.
4. Starting T_J = 25°C, L = 3.5mH, R_G = 25Ω, I_{AS} = -4.3A.
5. For PNP device voltage and current values will be negative (-).

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Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

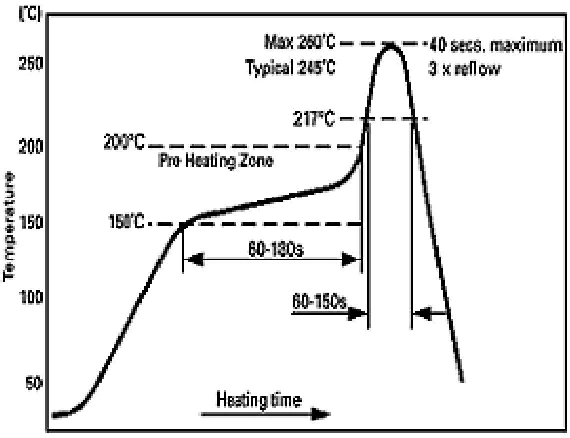
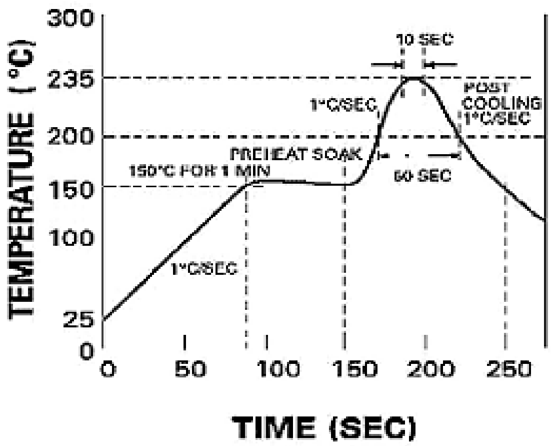


Figure 2



Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

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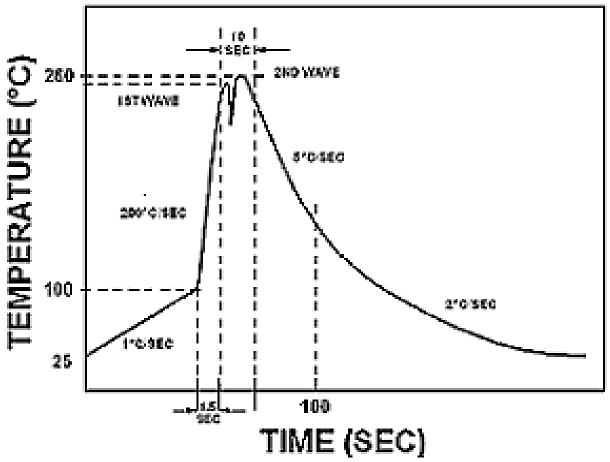
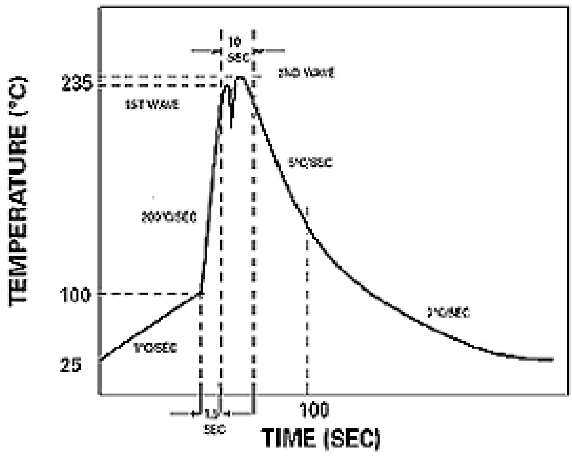
Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: Typical Output Characteristics

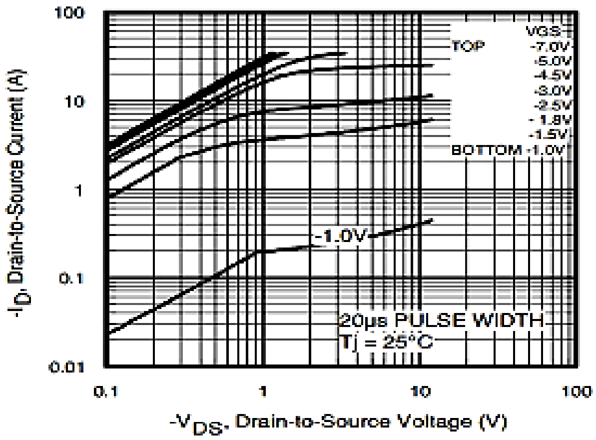


Fig 4: Typical Output Characteristics

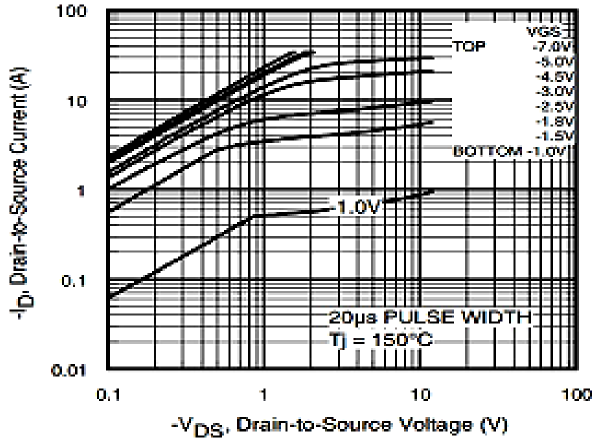


Fig 2: Typical Transfer Characteristics

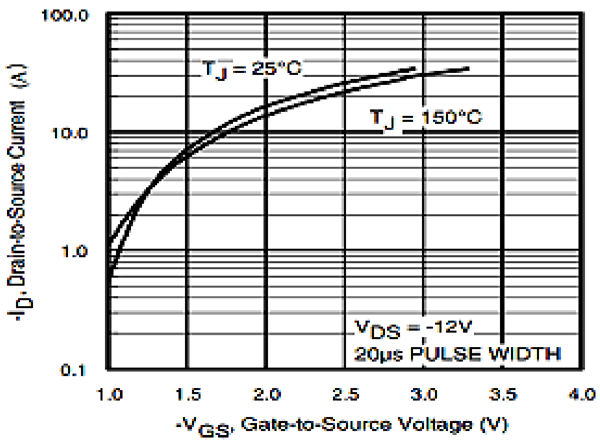


Fig 5: Normalized On-Resistance vs Temperature

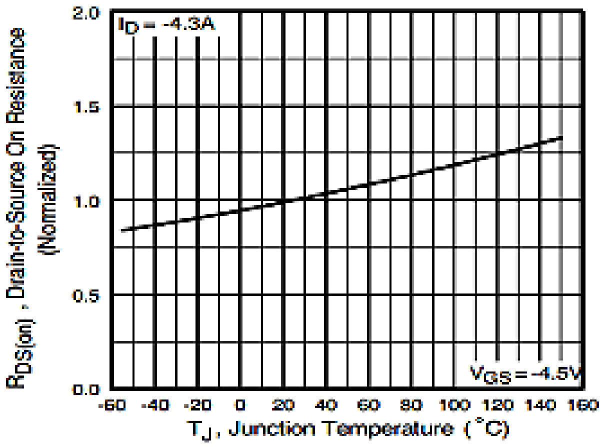


Fig 3: Typical Characteristics
vs Drain-to-source Voltage

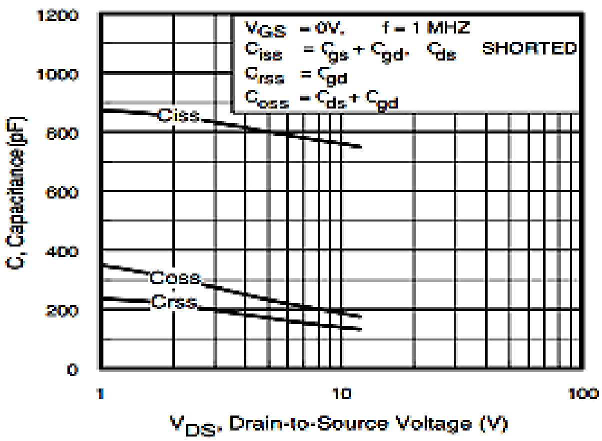
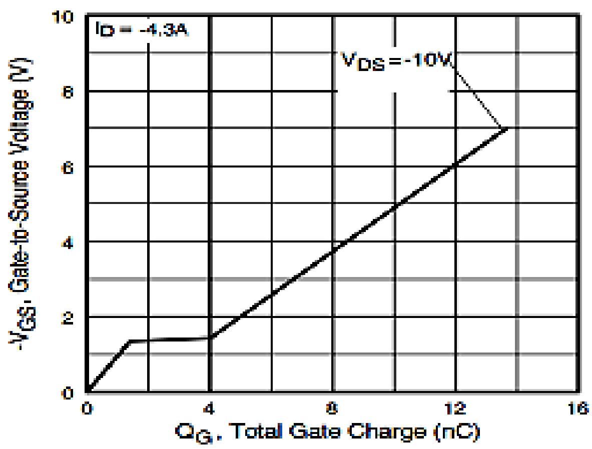


Fig 6: Typical Gate Charge
vs Gate-to-source Voltage



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TYPICAL CHARACTERISTICS CURVES

Fig 7: Typical Source-Drain Diode Forward Voltage

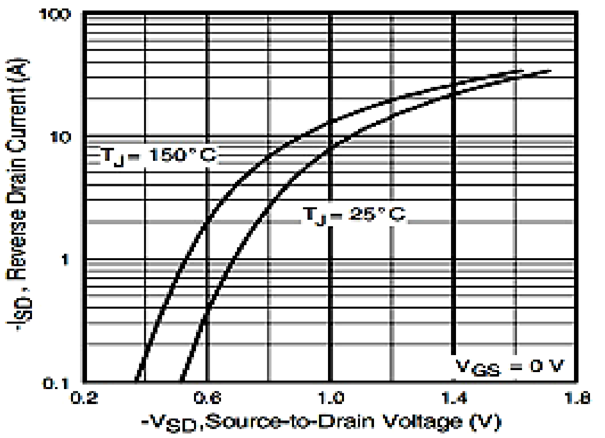


Fig 10: Maximum Safe Operating Area

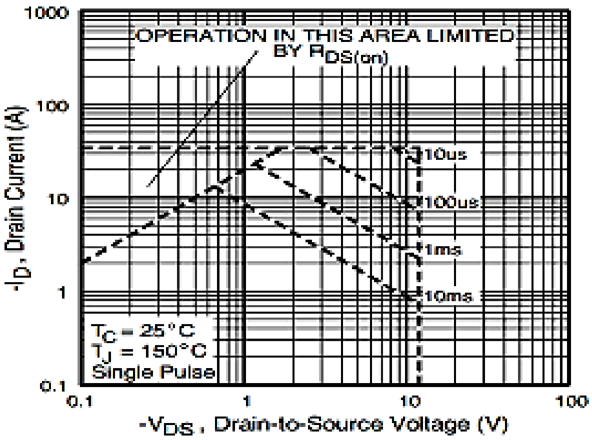


Fig 8: Maximum Drain Current
vs Case Temperature

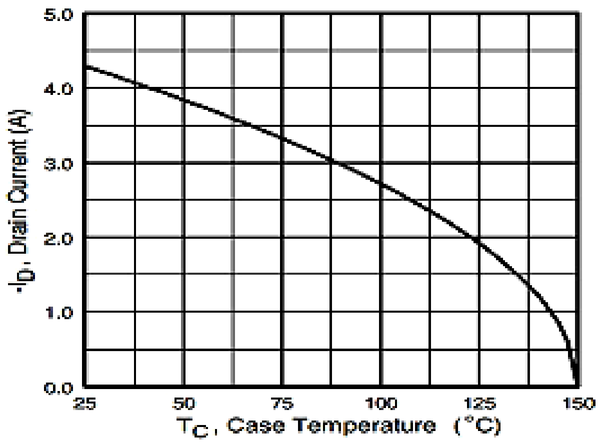


Fig 11: Maximum Avalanche Energy
vs Drain Current

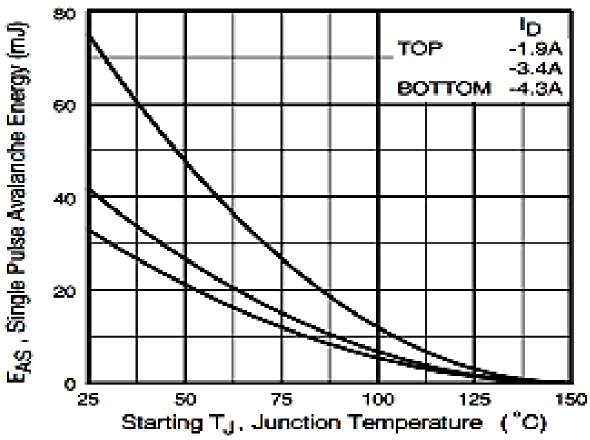


Fig 9: Typical On-Resistance vs Gate Voltage

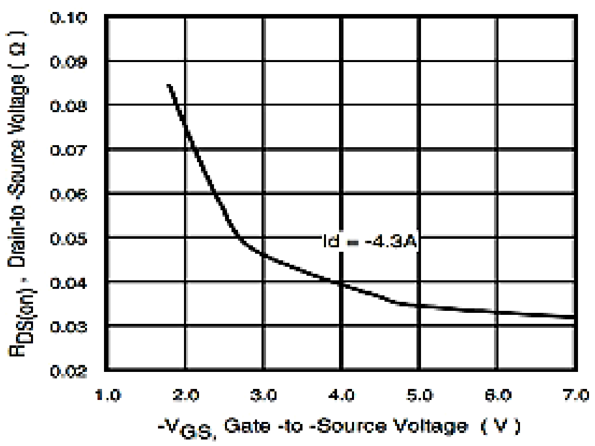
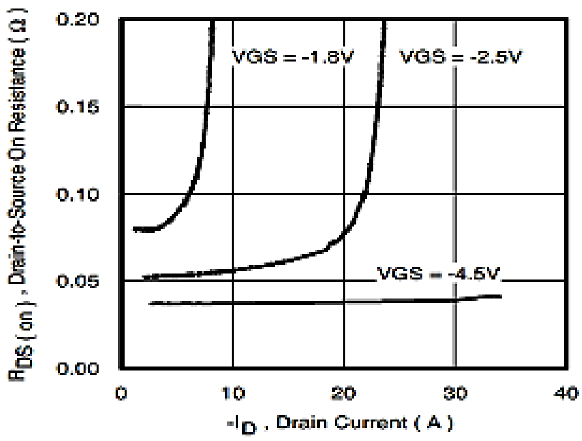


Fig 12: Typical On-Resistance vs Drain Voltage



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TYPICAL CHARACTERISTICS CURVES

Fig 13: Typical Threshold Voltage
vs Junctions Temperature

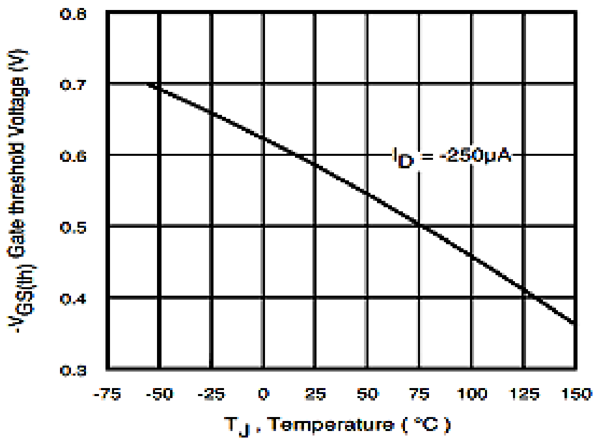
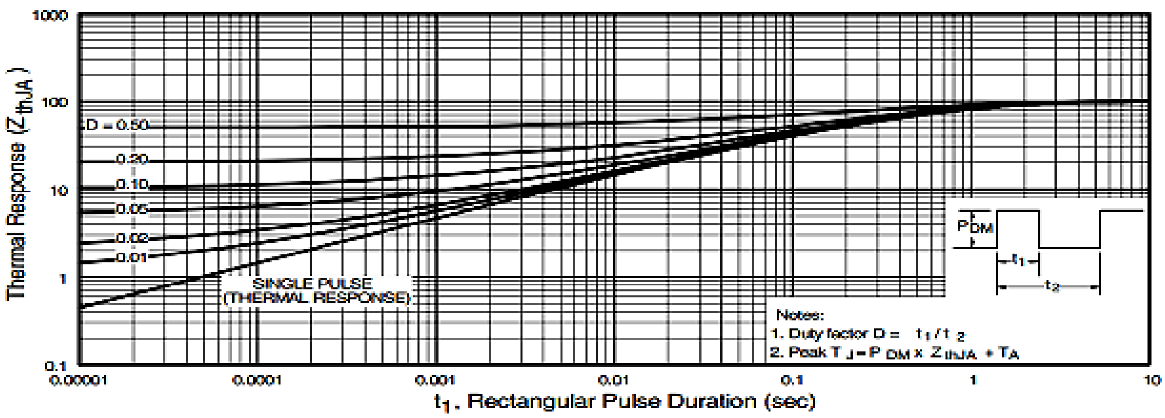
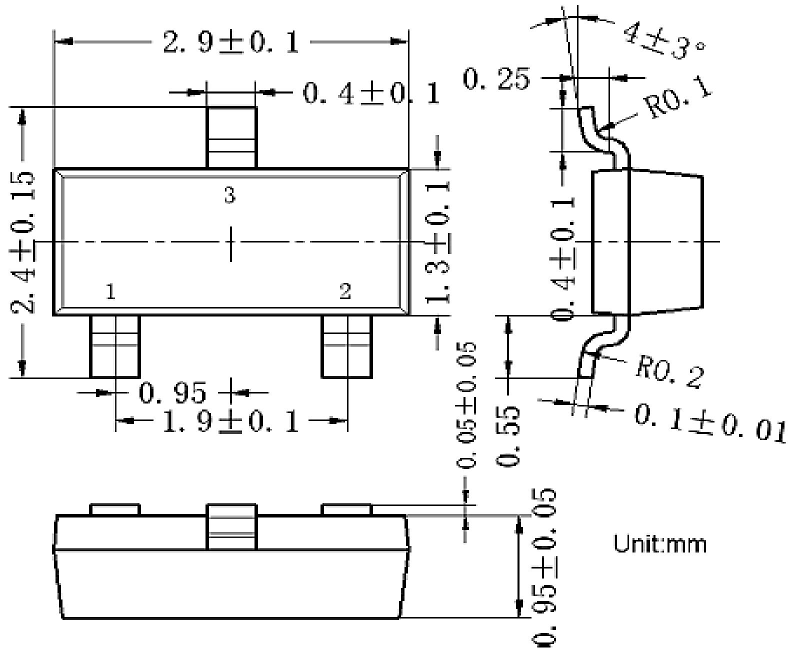


Fig 14: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



PACKAGE DETAILS

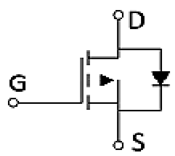
SOT-23 Leaded Plastic Package



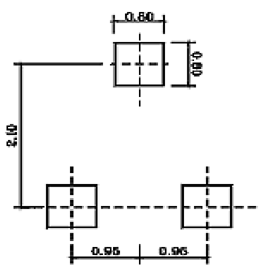
All Dimensions are in mm

Pin Configuration

1. Gate
2. Source
3. Drain



SOT-23 Suggested Pad Layout



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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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