



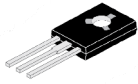
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NPN SILICON POWER TRANSISTORS

CSD882



TO-126

**TO-126 Leaded
Plastic Package
RoHS compliant**

Complementary CSB772

GENERAL DISCRIPTION:

The CSD882 is NPN Silicone Transistor suited for the Output Stage of 3 watt audio amplifier, Voltage regulator, DC-DC converter and relay driver.

FEATURES:

1. Low Saturation Voltage:
 $V_{CE(sat)} \cong 0.5V$ (@ $I_C = 2A, I_B = 0.2A$)
2. Excellent h_{FE} linearity and high h_{FE} .
 h_{FE} : 60 to 400 (@ $V_{CE} = 2V, I_C = 1A$)
3. Less Cramping space required due to small and think package and reducing the trouble for attachment to a radiator no insulator bushing required
4. This product is available in AEC-Q101 Qualified and PPAP Capable also.

Note: For AEC-Q101 qualified products, please use suffix -AQ in the part number while ordering.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT	
Maximum Temperature storage Temperature	T_{stg}	-55 to +150	°C	
Maximum Temperature Junction Temperature	T_j	150	°C	
Maximum Total power Dissipation	P_{tot}	$T_a = 25^\circ C$	1.0	W
		$T_c = 25^\circ C$	10	W
Collector to Base Voltage	V_{CBO}	40	V	
Collector to Emitter Voltage	V_{CEO}	30	V	
Emitter to Base Voltage	V_{EBO}	5.0	V	
Collector Current (DC)	$I_{C(DC)}$	3.0	A	
Collector Current (Pulse)	$I_{C(Pulse)}^1$	7.0	A	

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	Value			Unit
			Min.	Typ.	Max.	
DC Current Gain	h_{FE1}	$V_{CE} = 2.0\text{V}, I_C = 20\text{mA}^2$	30	150	--	
DC Current Gain	h_{FE2}	$V_{CE} = 2.0\text{V}, I_C = 1.0\text{A}^2$	60	160	400	
Gain Bandwidth Product	f_T	$V_{CE} = 5.0\text{V}, I_C = 0.1\text{A}$	--	90	--	MHz
Output Capacitance	C_{ob}	$V_{CB} = 10\text{V}, I_E = 0, f = \text{MHz}$	--	45	--	pF
Collector Cutoff Current	I_{CBO}	$V_{CB} = 30\text{V}, I_E = 0,$	--	--	1.0	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 3.0\text{V}, I_C = 0$	--	--	1.0	μA
Collector Saturation Voltage	$V_{CE(sat)}$	$I_C = 2.0\text{A}, I_B = 0.2\text{A}^2$	0.3	--	0.5	V
Base Saturation Voltage	$V_{BE(sat)}$	$I_C = 2.0\text{A}, I_B = 0.2\text{A}^2$	1.0	--	2.0	V

Classification of h_{FE}

Rank	R	Q	P	E
Range	60 to 120	100 to 200	160 to 320	200 to 400

Test Conditions: $V_{CE} = 2.0\text{V}, I_C = 1.0\text{A}$

Note:

1. Pulse test: $PW \cong 300\mu\text{s}$, duty cycle=2%
2. Pulse test: $PW \cong 350\mu\text{s}$, duty cycle=2%

TYPICAL CHARACTERISTICS CURVES

Fig 1: Total Power Dissipation vs Ambient Temp

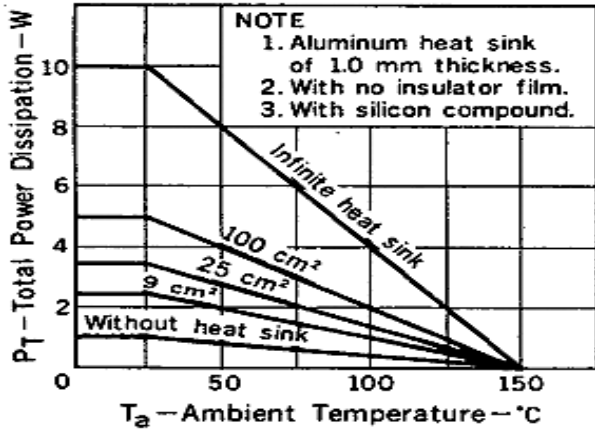


Fig 2: Thermal Resistance vs Pulse Width

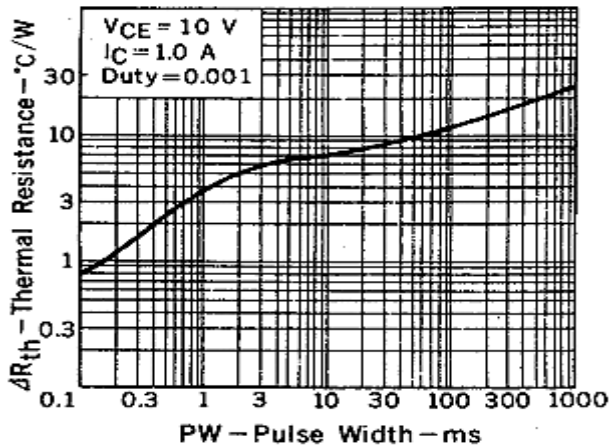


Fig 3: Collector Current vs Collector to Emitter Voltage

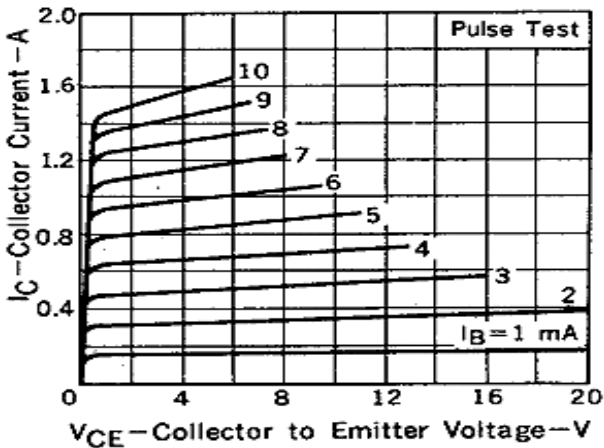


Fig 4: Derating Curves for all types

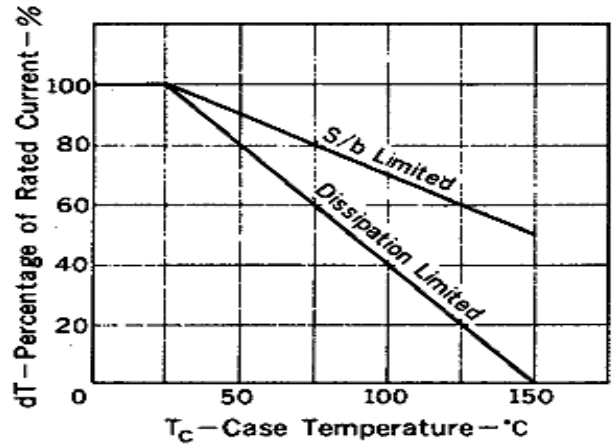


Fig 5: Safe Operating Areas

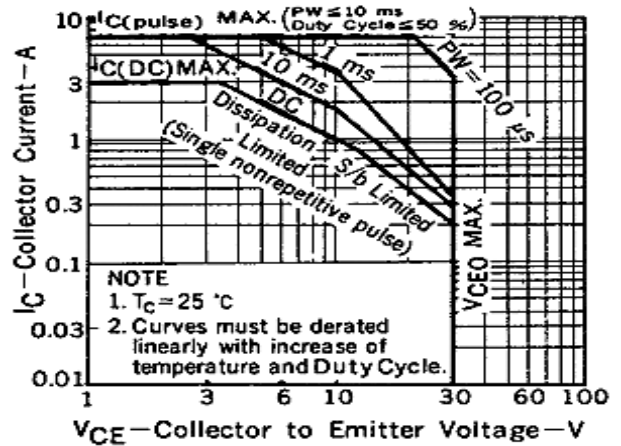
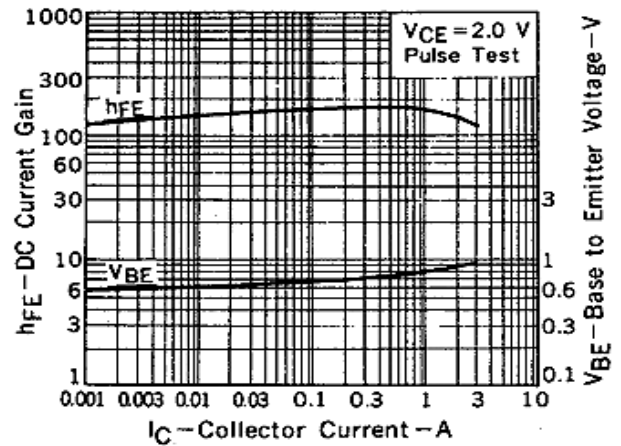


Fig 6: DC Current Gain Base to Emitter Voltage vs Collector Current



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TYPICAL CHARACTERISTICS CURVES

Fig 7: Base & Collector Saturation Voltage vs Collector Current

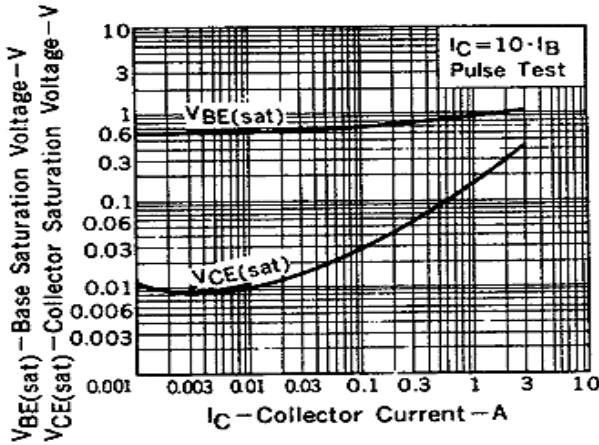


Fig 9: Gain Bandwidth Product vs Collector Current

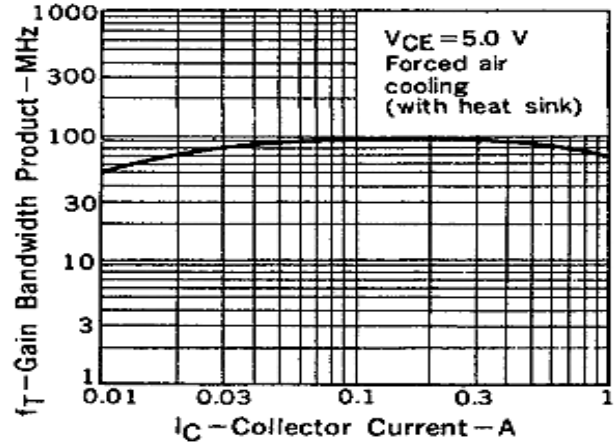
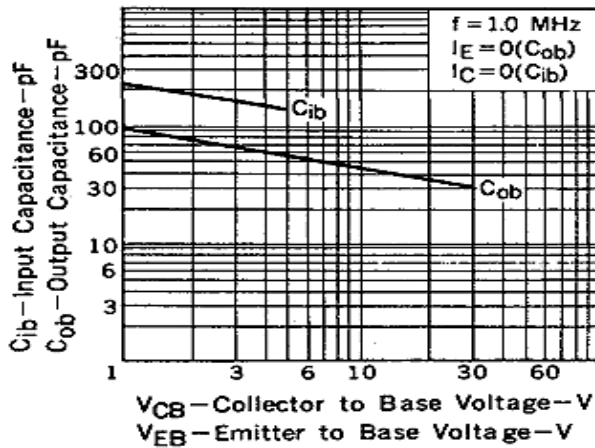


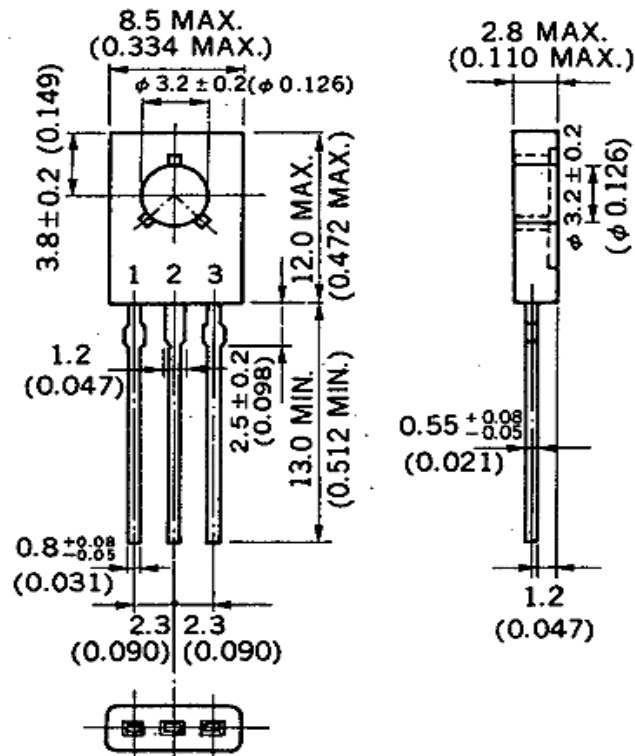
Fig 8: Input & Output Capacitance vs Reverse Voltage



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Package Details

TO-126 Leaded Plastic Package



All Dimensions are in Millimeter (Inches)

PIN CONFIGURATION

1. Emitter
2. Collector
3. Base

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

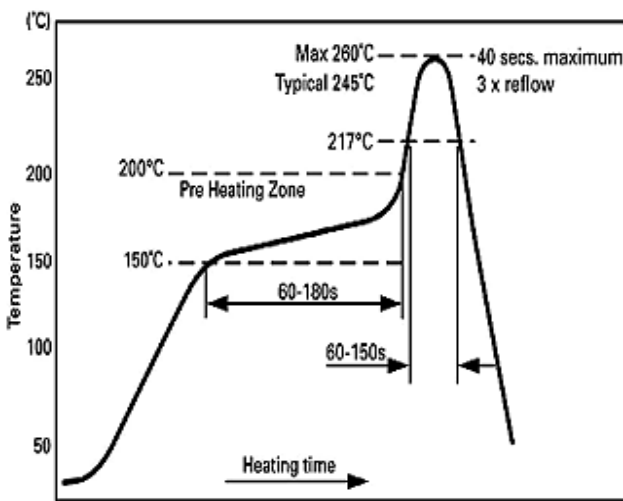
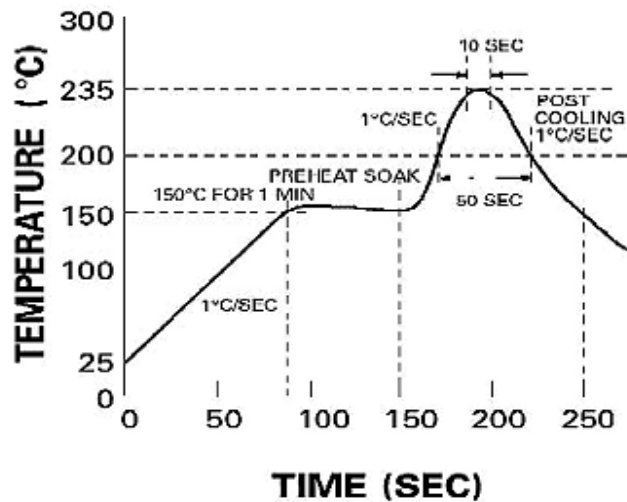


Figure 2



Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat		
– Temperature Range	150-170°C	150-200°C
– Time	60-180 seconds	60-180 seconds
Time maintained above:		
– Temperature	200°C	217°C
– Tim	30-50 seconds	60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max



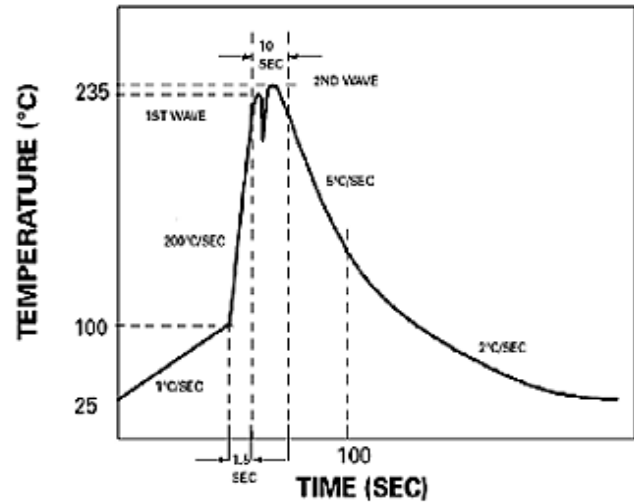
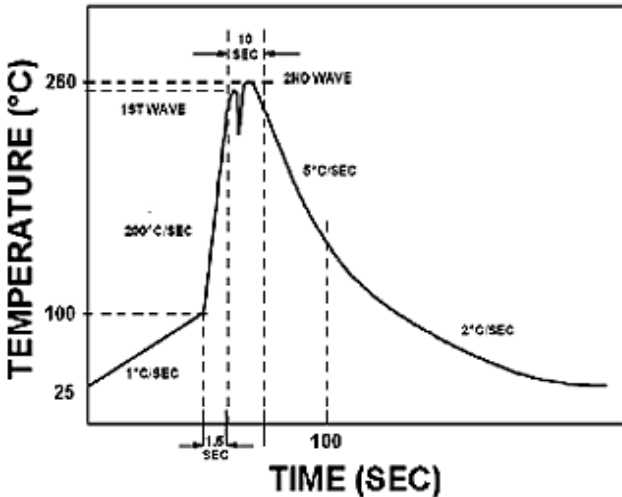
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Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free The Recommended solder Profile For Devices



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

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Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the Coil's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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