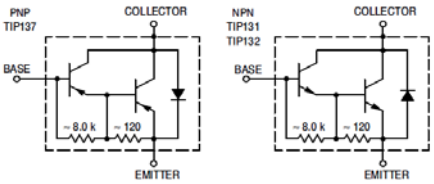
# Darlington Complementary Silicon Power Transistors

| NPN | PNP |
|---|---|
| TIP130 | TIP135 |
| TIP131 | TIP136 |
| TIP132 | TIP137 |

TO-220




Darlington Circuit Schematic

**TO-220**
**Plastic Package**
**RoHS compliant**

## FEATURES:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

**Note:** For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

**APPLICATIONS:** Intended for use in Linear and Switching Applications

## ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

| PARAMETER | SYMBOL | TIP130/135 | TIP131/136 | TIP132/137 | UNIT |
|---|---|---|---|---|---|
| Collector Emitter Voltage | $V_{CEO}$ | 60 | 80 | 100 | V |
| Collector Base Voltage | $V_{CBO}$ | 60 | 80 | 100 | V |
| Emitter Base Voltage | $V_{EBO}$ | 5.0 | | | V |
| Collector Current Continuous | $I_C$ | 8.0 | | | A |
| Collector Current Peak | $I_{CM}$ | 12 | | | A |
| Base Current | $I_B$ | 0.3 | | | A |
| Power Dissipation upto Tc=25ºC | $P_D$ | 70 | | | W |
| Power Dissipation upto Ta=25ºC | $P_D$ | 2.0 | | | W |
| Derate above 25ºC | | 16 | | | mW/°C |
| Operating And Storage Junction Temperature | $T_j$, $T_{stg}$ | -65 to +150 | | | °C |
| Junction to Case | $R_{th\ (j\text{-}c)}$ | 1.78 | | | °C/W |
| Junction to Ambient in free air | $R_{th\ (j\text{-}a)}$ | 62.5 | | | °C/W |

## ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise

| PARAMETER | SYMBOL | TEST CONDITION | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Collector Cut off Current | $I_{CEO}$ | $V_{CE}$= Half Rated $V_{CEO}$ | | -- | -- | 0.5 | mA |
| Collector Cut off Current | $I_{CBO}$ | $V_{CB}$= Rated $V_{CBO}$ | | -- | -- | 0.2 | mA |
| Emitter Cut off Current | $I_{EBO}$ | $V_{EB}$=5V, $I_C$=0 | | -- | -- | 5.0 | mA |
| Collector Emitter (sus) Voltage | $V_{CEO(sus)}$ [1] | $I_C$=30mA, $I_B$=0 | TIP130/135 | 60 | -- | -- | V |
| | | | TIP131/136 | 80 | -- | -- | V |
| | | | TIP132/137 | 100 | -- | -- | V |
| Collector Emitter Saturation Voltage | $V_{CE\ (sat)}$ [1] | $I_C$=4A, $I_B$=16mA | | -- | -- | 2.0 | V |
| | | $I_C$=6A, $I_B$=30mA | | -- | -- | 3.0 | V |
| Base Emitter on Voltage | $V_{BE(on)}$ [1] | $I_C$=4A, $V_{CE}$=4V | | -- | -- | 2.5 | V |
| DC Current Gain | $h_{FE}$ [1] | $I_C$=1A, $V_{CE}$=4V | | 500 | -- | -- | |
| | | $I_C$=4A, $V_{CE}$=4V | | 1000 | -- | 15000 | |

**Note:**

1. Pulse Test : Pulse width≤300µs, Duty Cycle ≤2%

TIP130_137
Rev02_ 13062022E

## Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

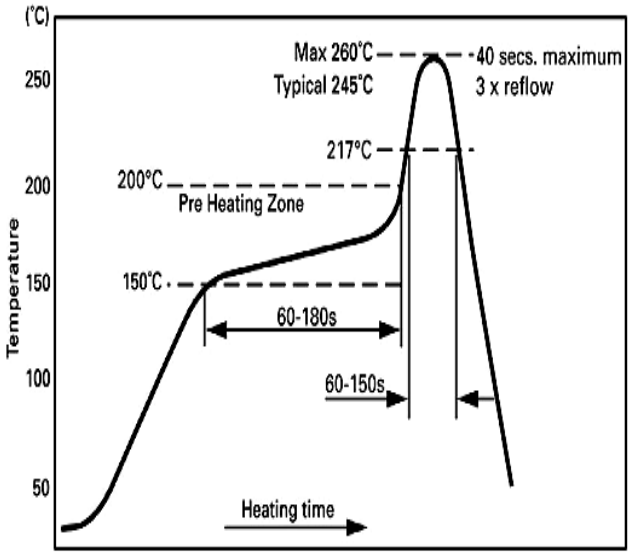
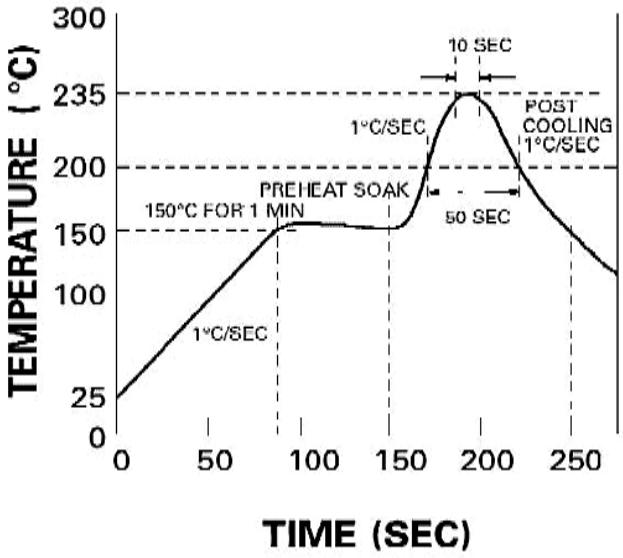



Figure 2

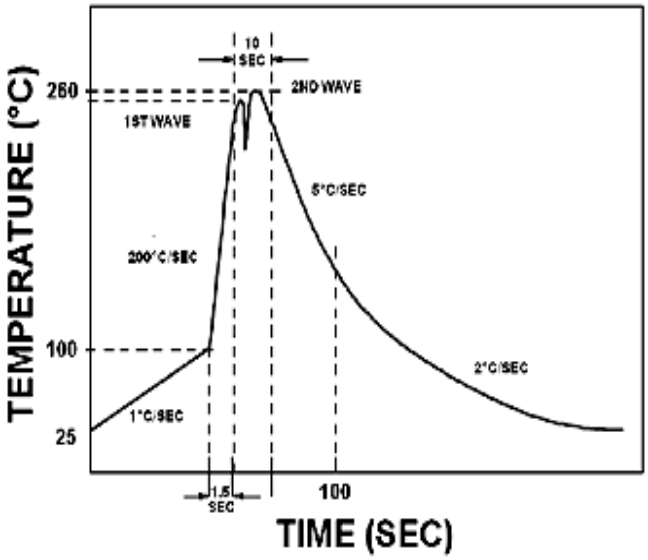



**Reflow profiles in tabular form**

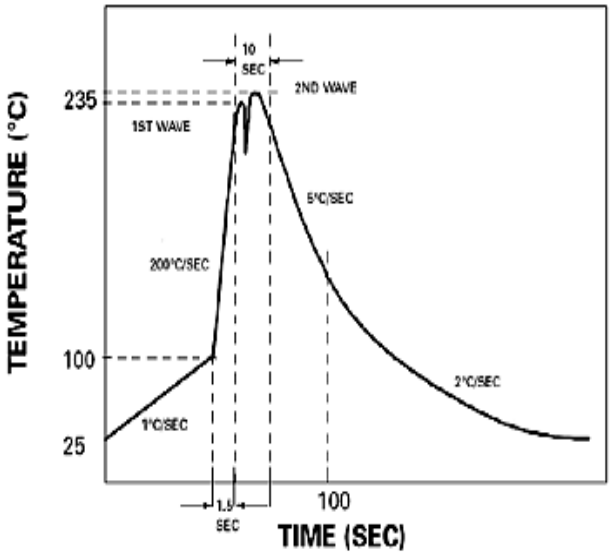
| Profile Feature | Sn-Pb System | Pb-Free System |
|---|---|---|
| Average Ramp-Up Rate | ~3°C/second | ~3°C/second |
| **Preheat**<br>– Temperature Range<br>– Time | <br>150-170°C<br>60-180 seconds | <br>150-200°C<br>60-180 seconds |
| Time maintained above:<br>– Temperature<br>– Time | <br>200°C<br>30-50 seconds | <br>217°C<br>60-150 seconds |
| Peak Temperature | 235°C | 260°C max. |
| Time within +0 -5°C of actual Peak | 10 seconds | 40 seconds |
| Ramp-Down Rate | 3°C/second max. | 6°C/second max. |

## Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used




The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder




### Wave Profiles in Tabular Form

| Profile Feature | Sn-Pb System | Pb-free System |
|---|---|---|
| Average Ramp-Up Rate | ~200°C/second | ~200°C/second |
| Heating rate during preheat | Typical 1-2, Max 4°C/sec | Typical 1-2, Max 4°C/Sec |
| Final preheat Temperature | Within 125°C of Solder Temp | Within 125°C of Solder Temp |
| Peak Temperature | 235°C | 260°C max. |
| Time within +0 -5°C of actual Peak | 10 seconds | 10 seconds |
| Ramp-Down Rate | 5°C/second max. | 5°C/second max |

Figure 1. Power Derating

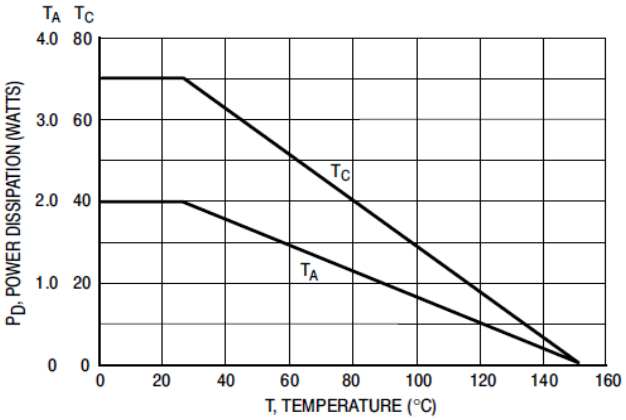
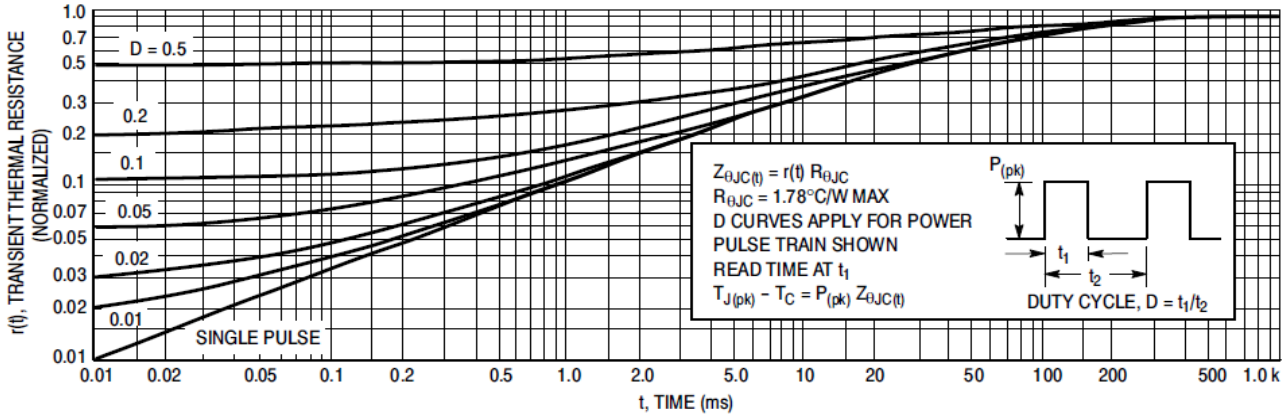
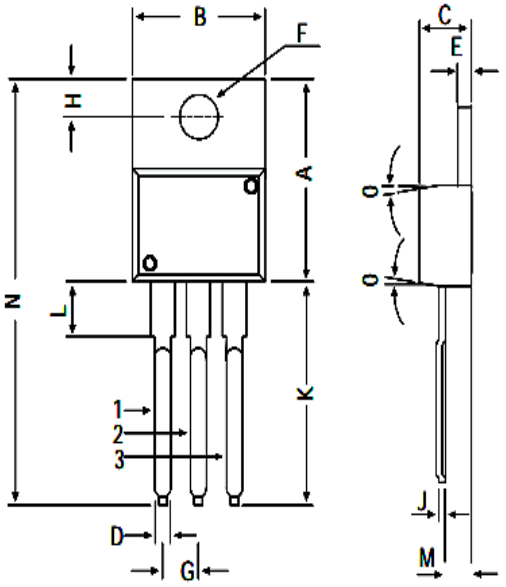



Figure 2. Thermal Response



## PACKAGE DETAILS

TO-220 Plastic Package

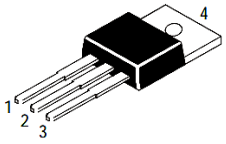



| DIM | MIN | MAX |
|---|---|---|
| A | 14.42 | 16.51 |
| B | 9.63 | 10.67 |
| C | 3.56 | 4.83 |
| D | -- | 0.90 |
| E | 1.15 | 1.40 |
| F | 3.75 | 3.88 |
| G | 2.29 | 2.79 |
| H | 2.54 | 3.43 |
| J | -- | 0.56 |
| K | 12.70 | 14.73 |
| L | 2.8 | 4.07 |
| M | 2.03 | 2.92 |
| N | -- | 31.24 |
| O | 7 DEG | |

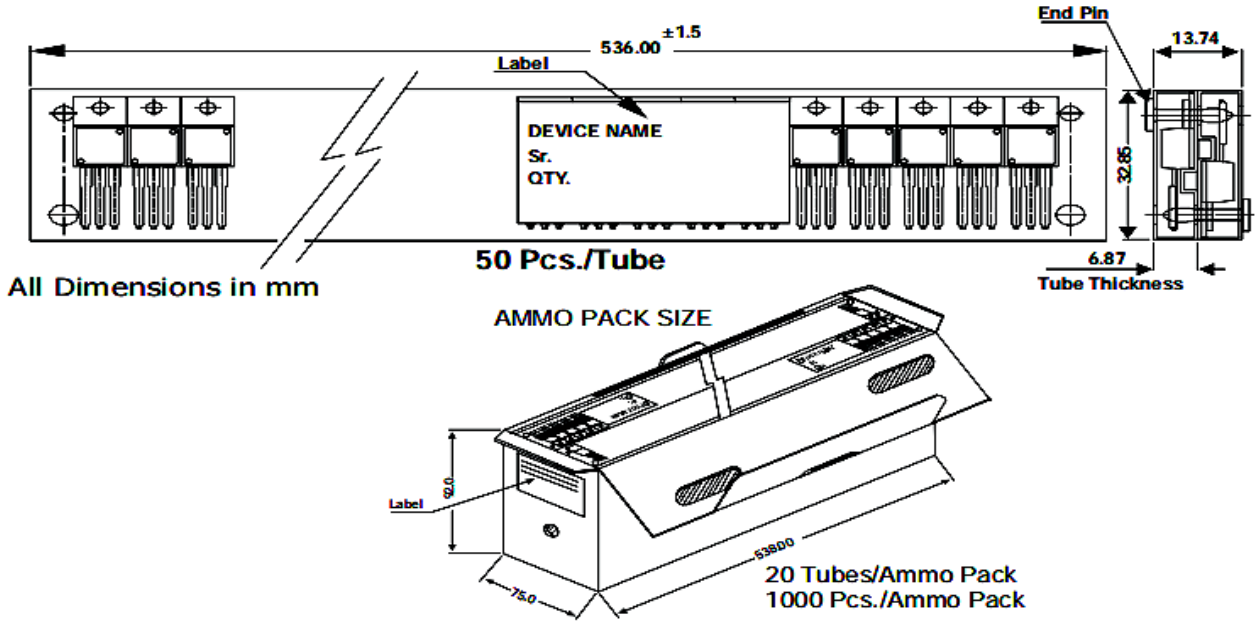
All diminsions in mm.

**Pin Configuration**

1. Base
2. Collector
3. Emitter
4. Collector



## TO-220 Tube Packing




## Packing Detail

| PACKAGE | STANDARD PACK | | INNER CARTON BOX | | OUTER CARTON BOX | | |
|---|---|---|---|---|---|---|---|
| | Details | Net Weight/Qty | Size | Qty | Size | Qty | Gr Wt |
| TO-220 | 200 pcs/polybag | 396 gm/200 pcs | 3" x 7.5" x 7.5" | 1.0K | 17" x 15" x 13.5" | 16.0K | 36 kgs |
| | 50 pcs/tube | 120 gm/50 pcs | 3.5" x 3.7" x 21.5" | 1.0K | 19" x 19" x 19" | 10.0K | 29 kgs |

# Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

## Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

## Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

| JEDEC MSL Level | | |
|---|---|---|
| **Level** | **Time** | **Condition** |
| 1 | Unlimited | ≤30 °C / 85% RH |
| 2 | 1 Year | ≤30 °C / 60% RH |
| 2a | 4 Weeks | ≤30 °C / 60% RH |
| 3 | 168 Hours | ≤30 °C / 60% RH |
| 4 | 72 Hours | ≤30 °C / 60% RH |
| 5 | 48 Hours | ≤30 °C / 60% RH |
| 5a | 24 Hours | ≤30 °C / 60% RH |
| 6 | Time on Label(TOL) | ≤30 °C / 60% RH |

## Customer Notes

**Component Disposal Instructions**

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

## Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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